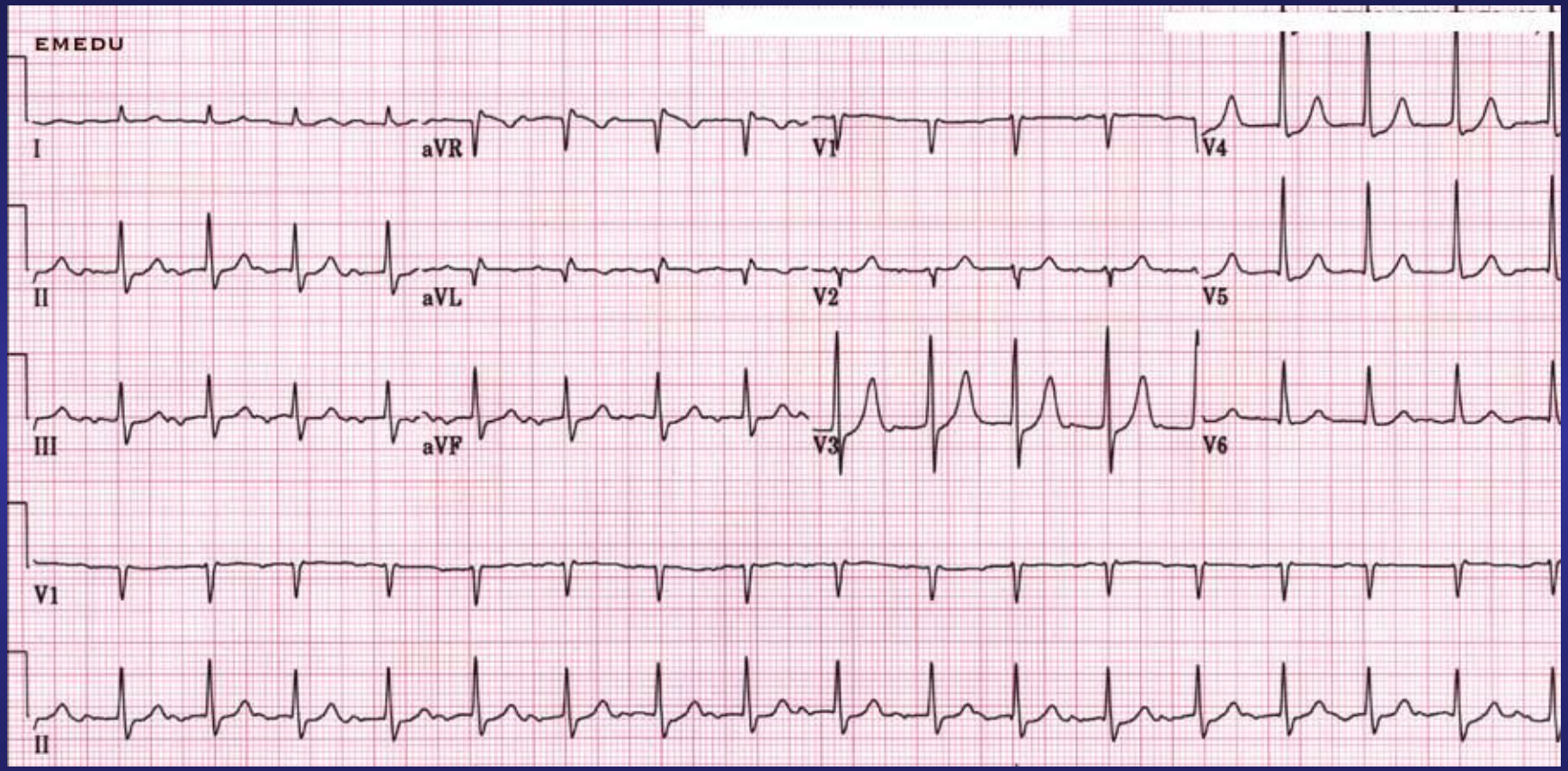
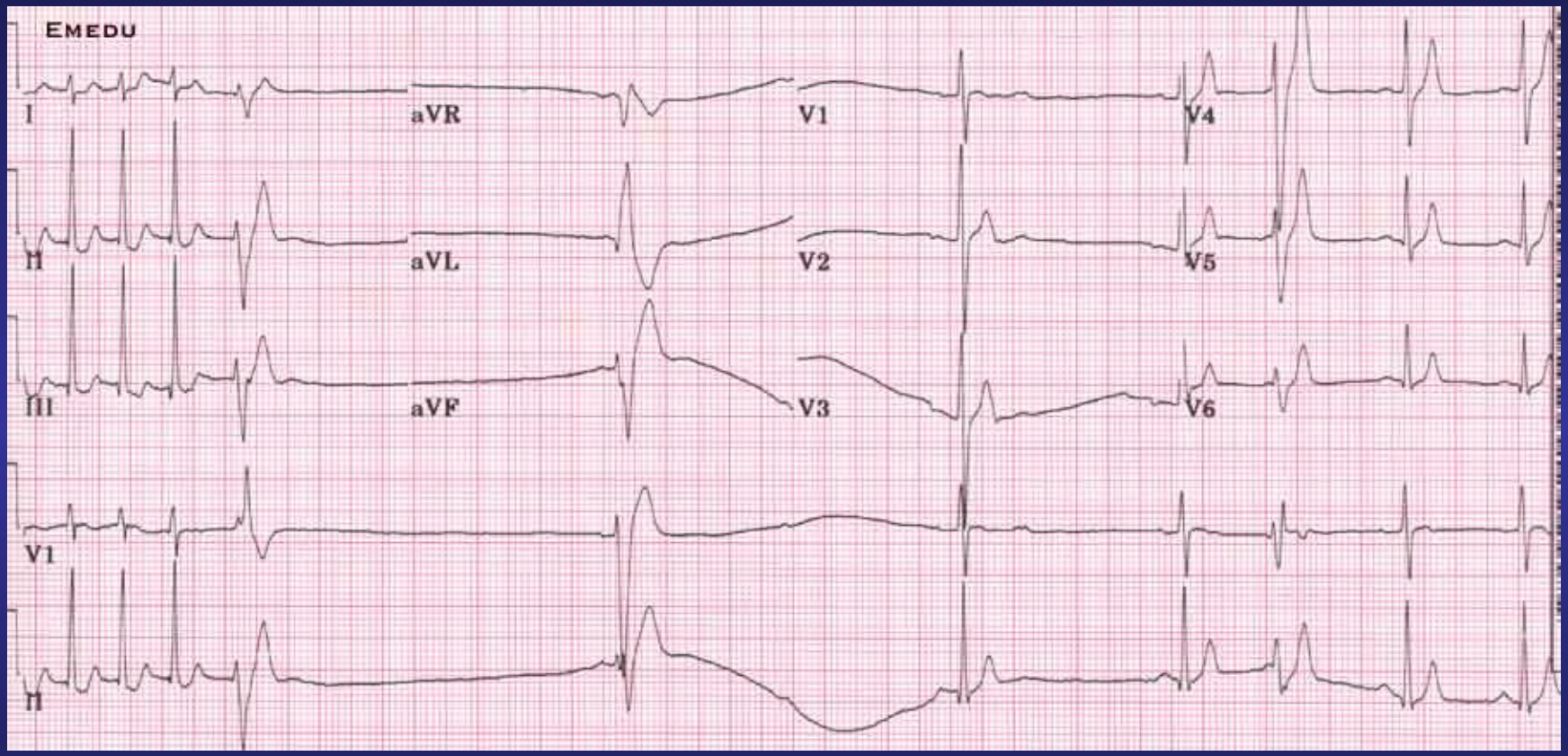
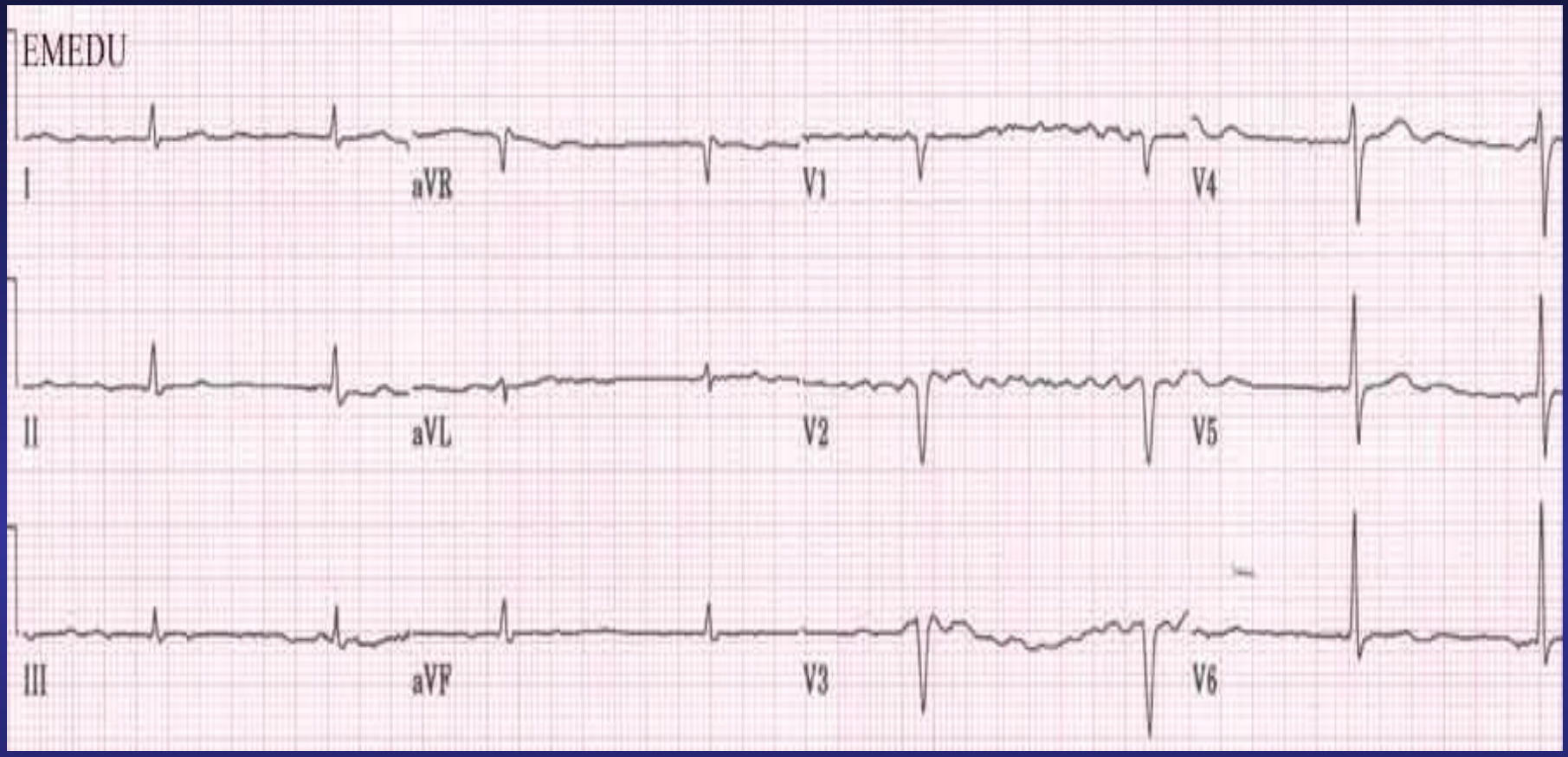
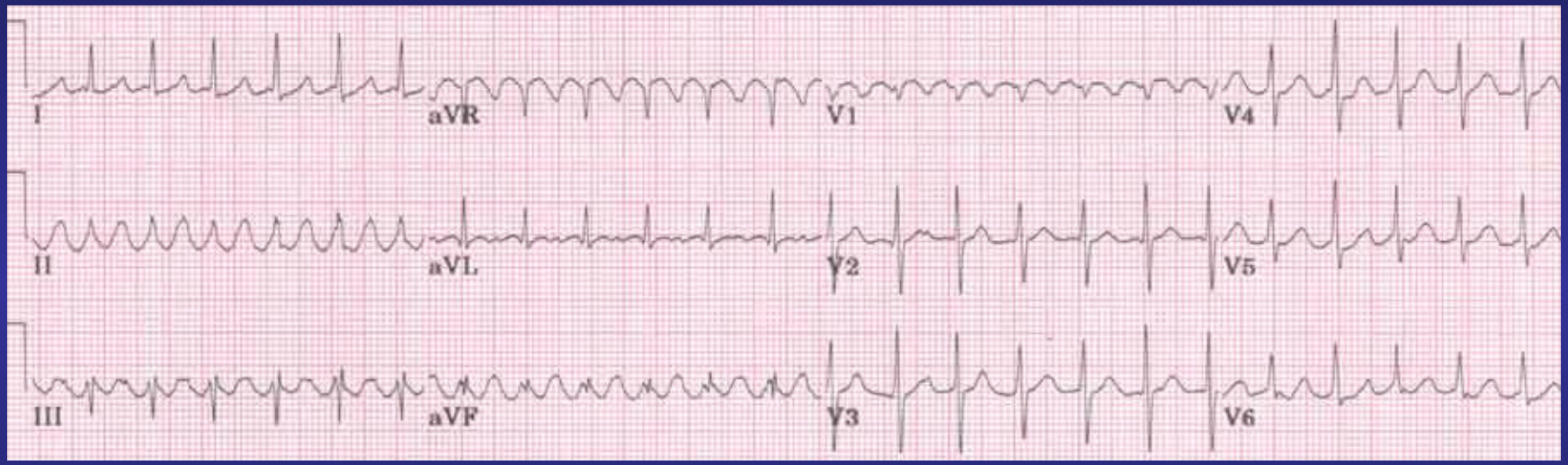
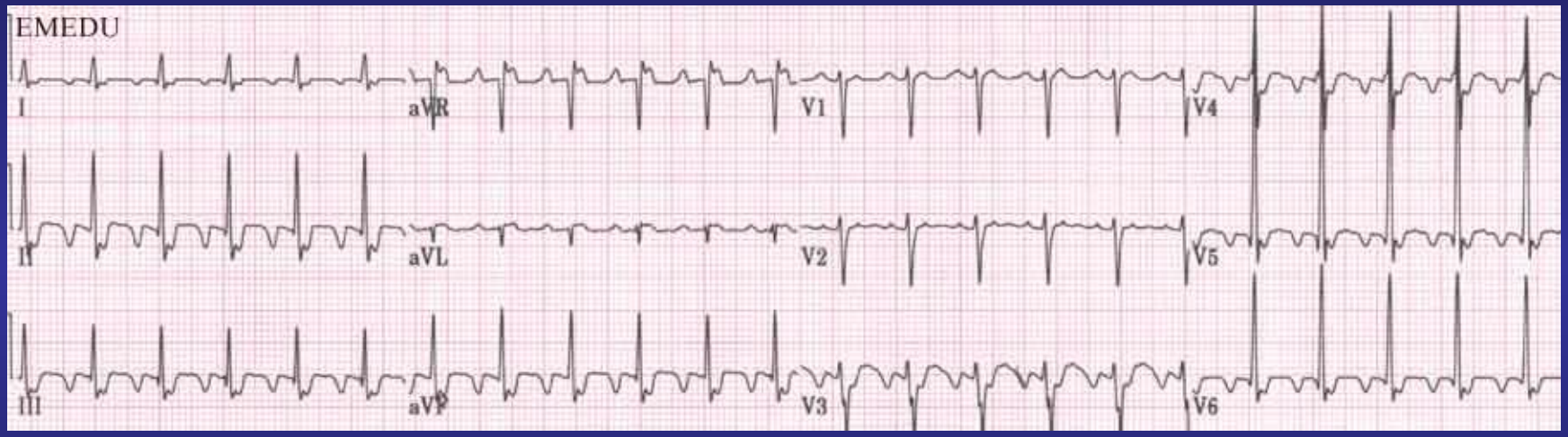
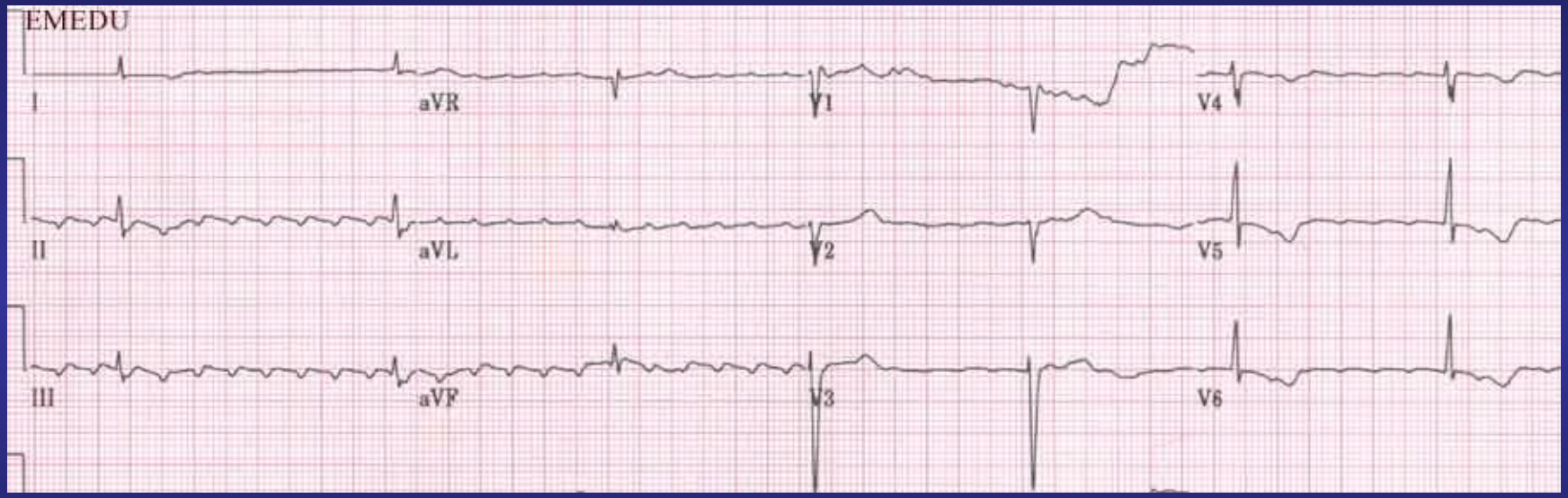

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6
V1
II

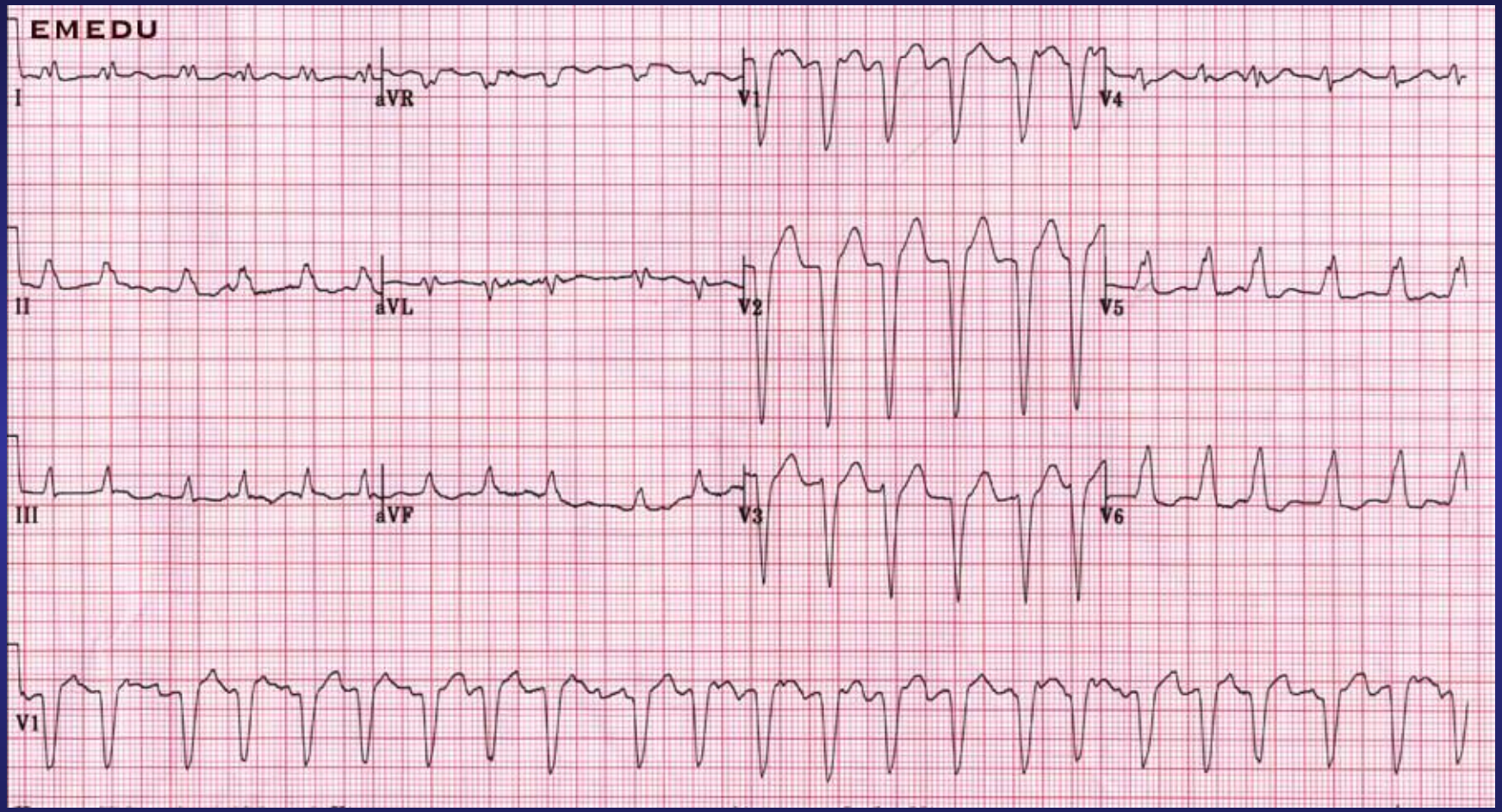

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6
V1
II

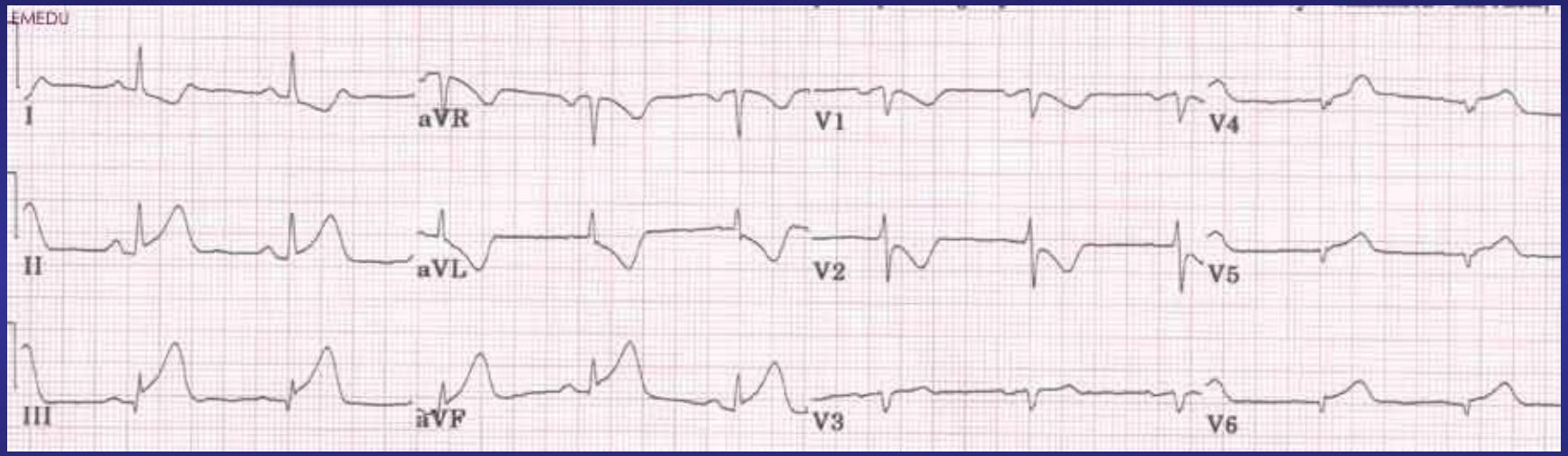

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6

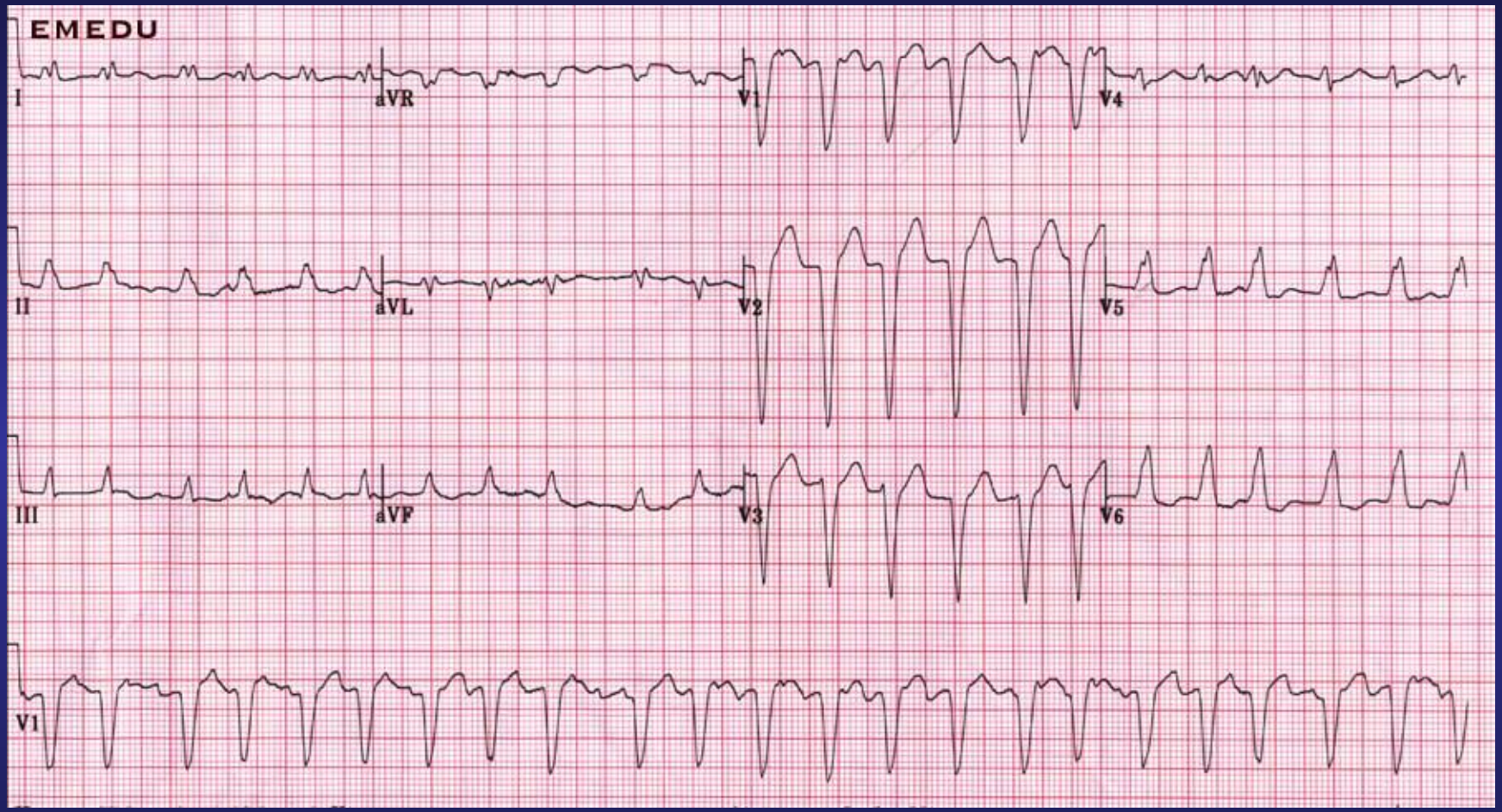

I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6

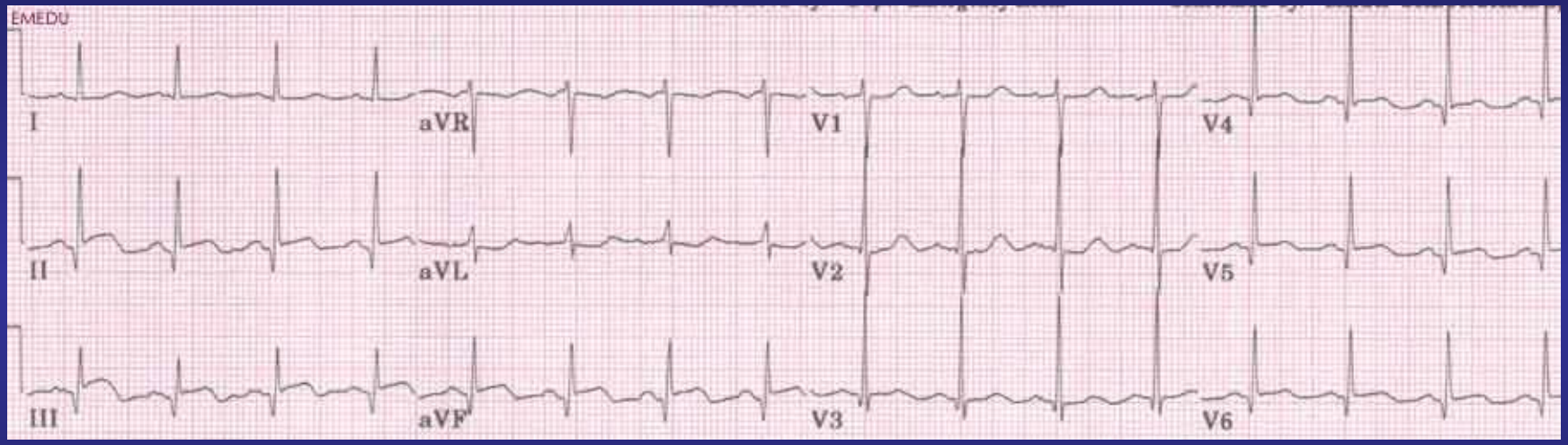

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6

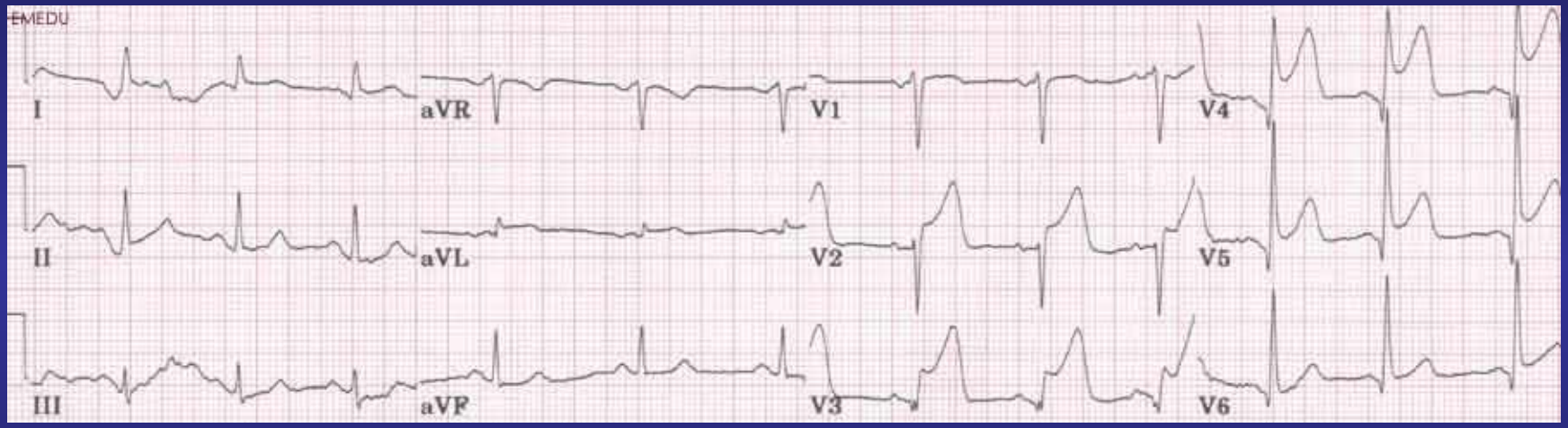

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6

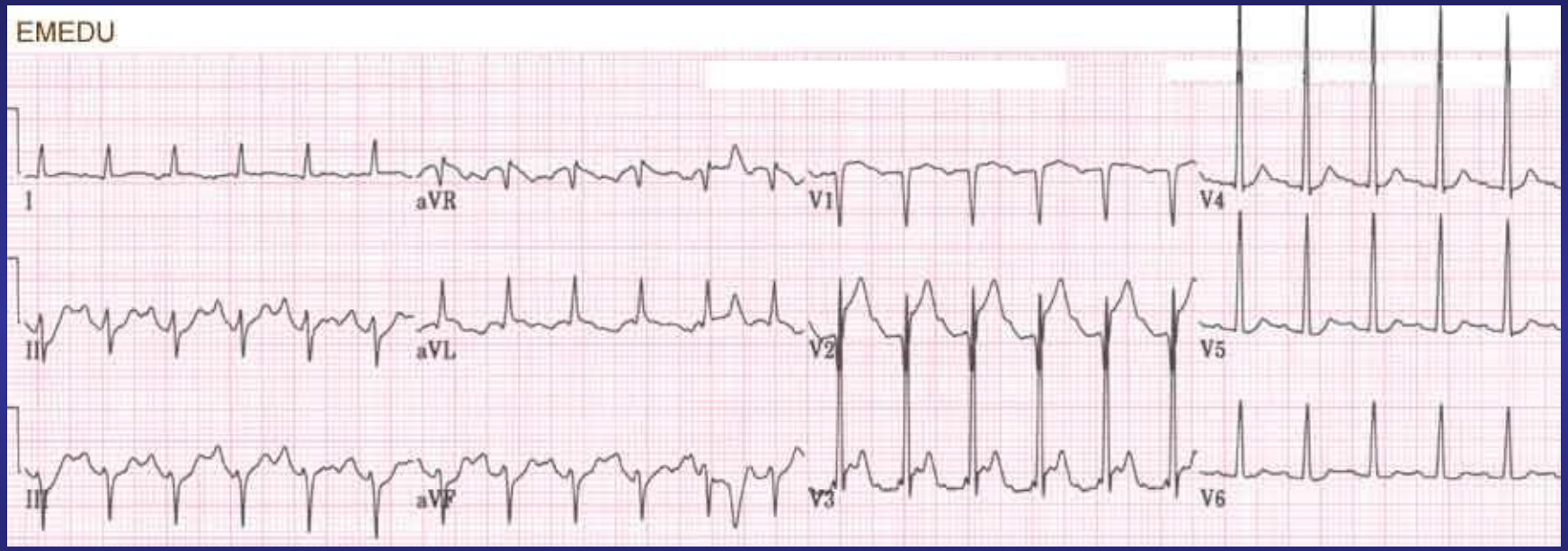

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6
V1

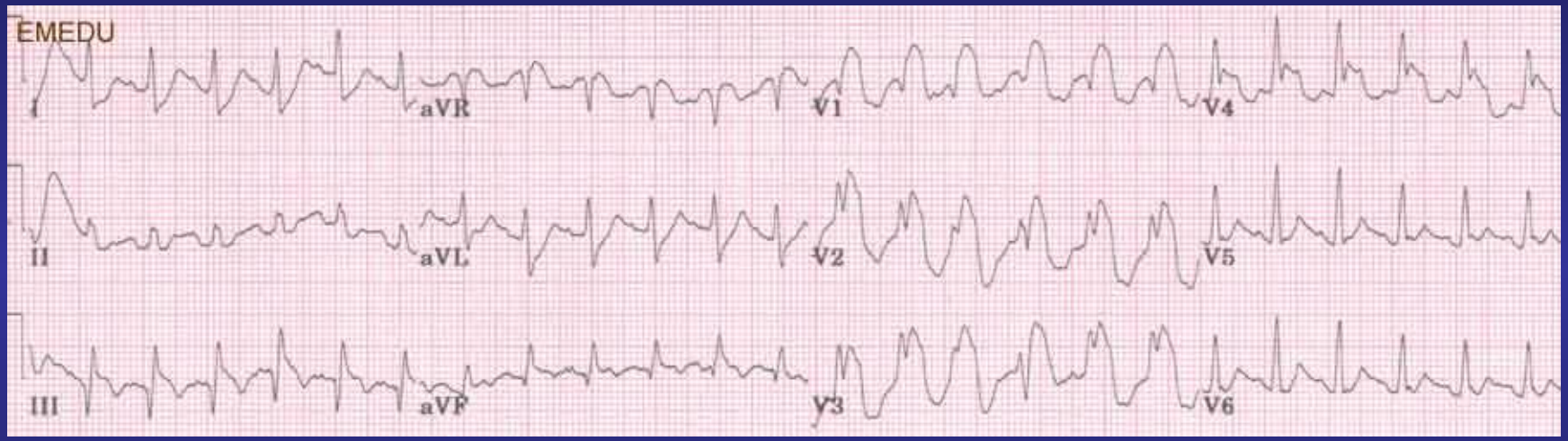

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6

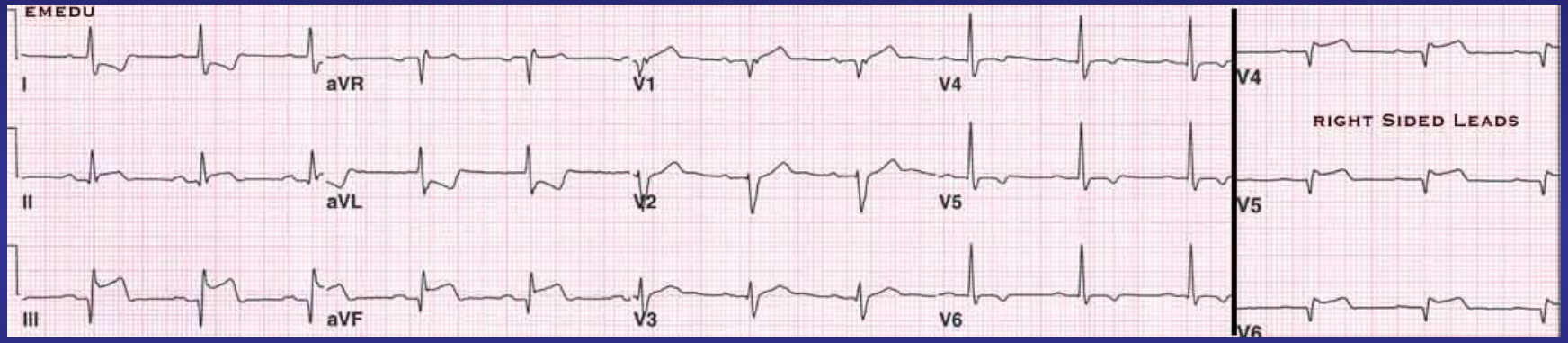

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6
V1

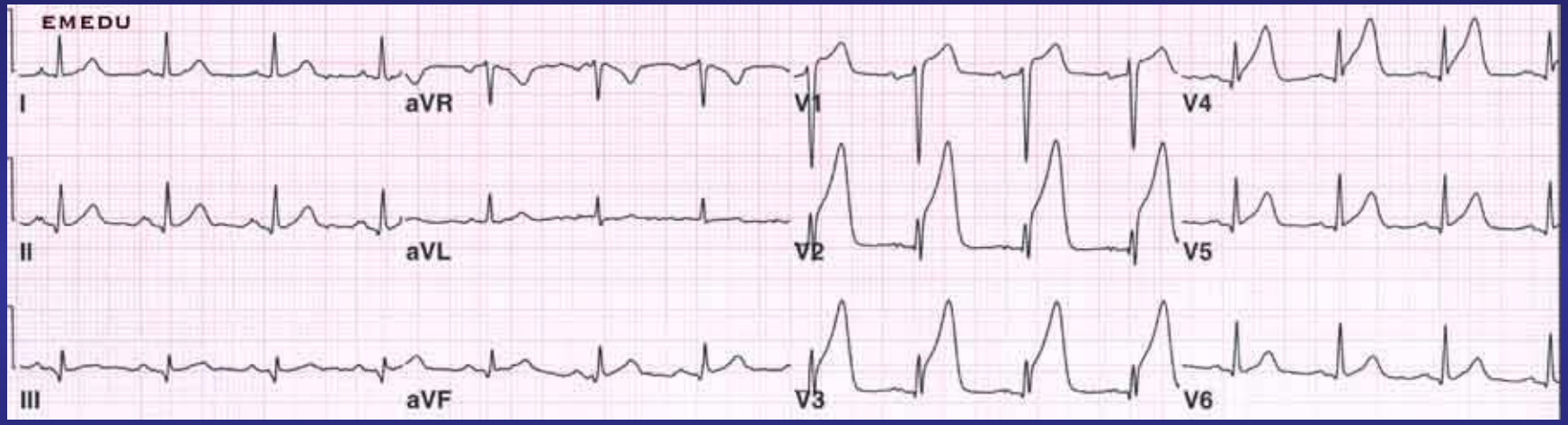

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6

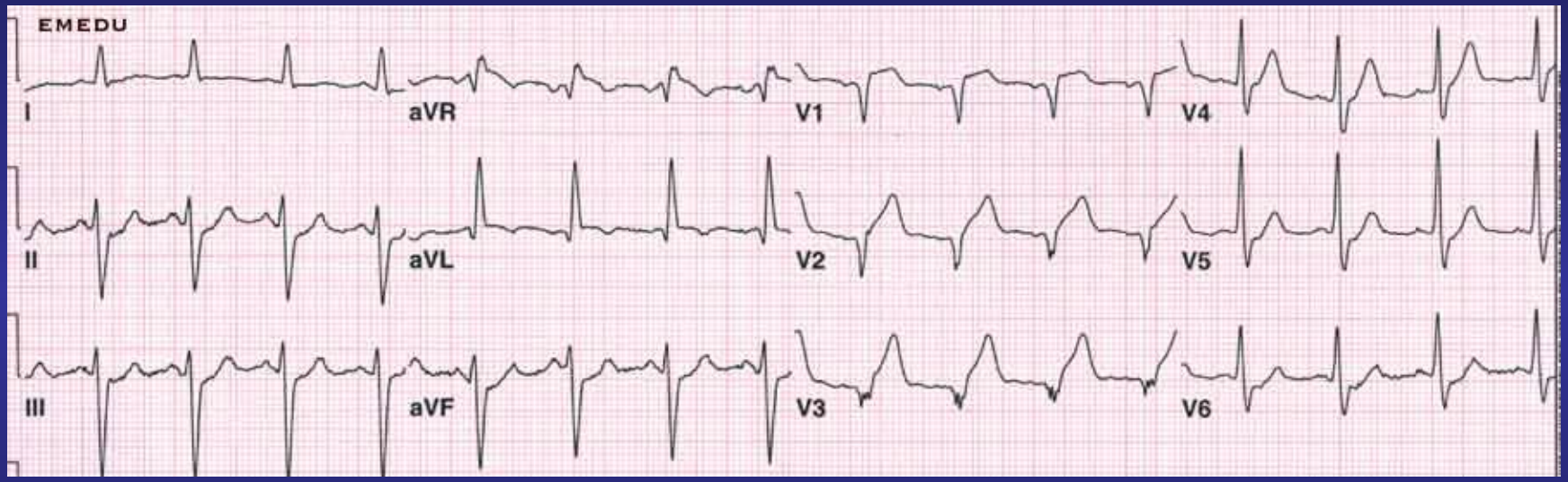

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6

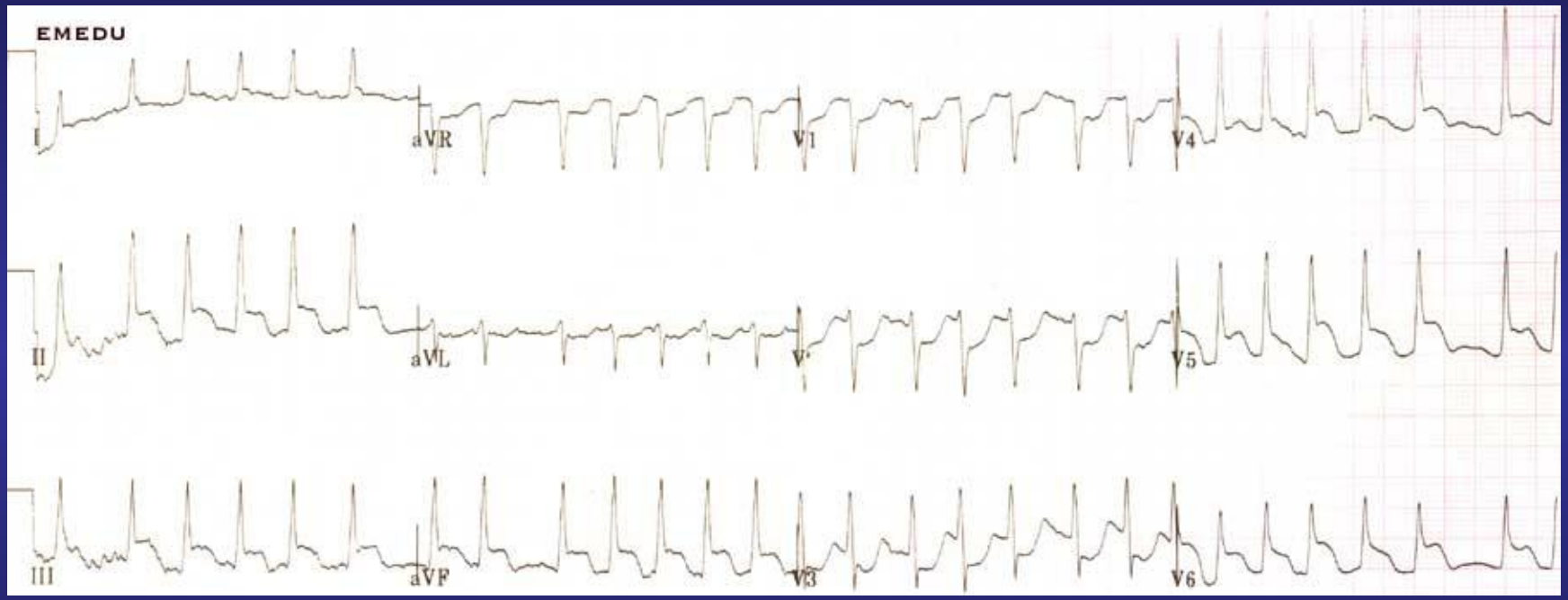

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6

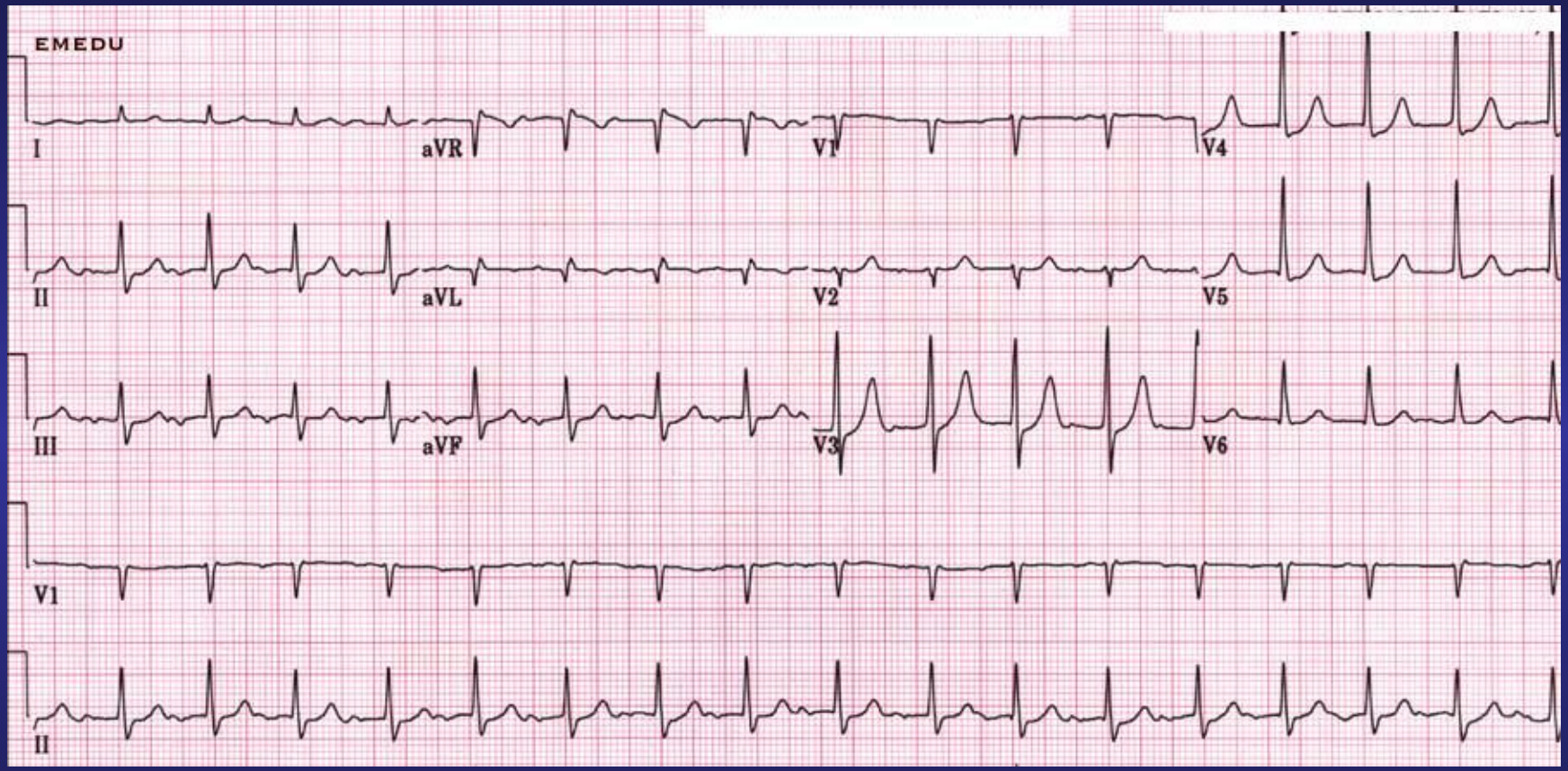

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6

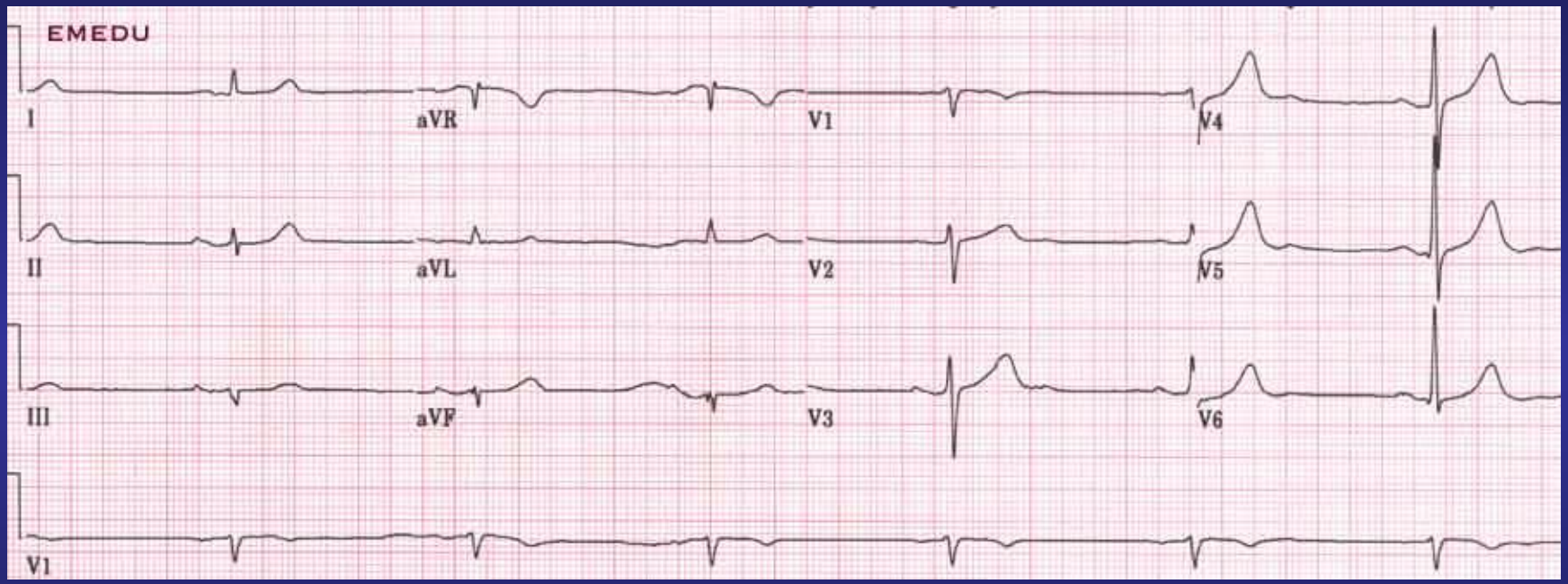

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6
V4
RIGHT SIDED LEADS
V5
V6

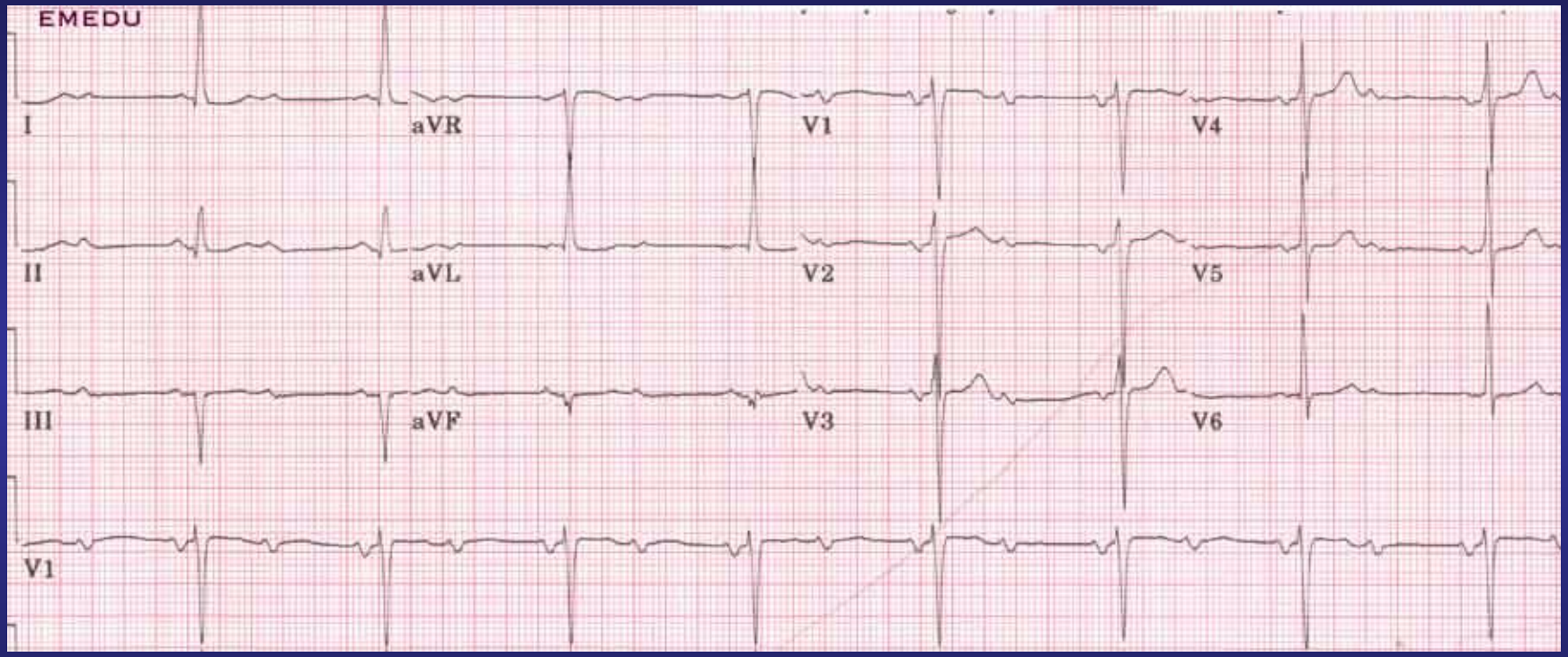

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6

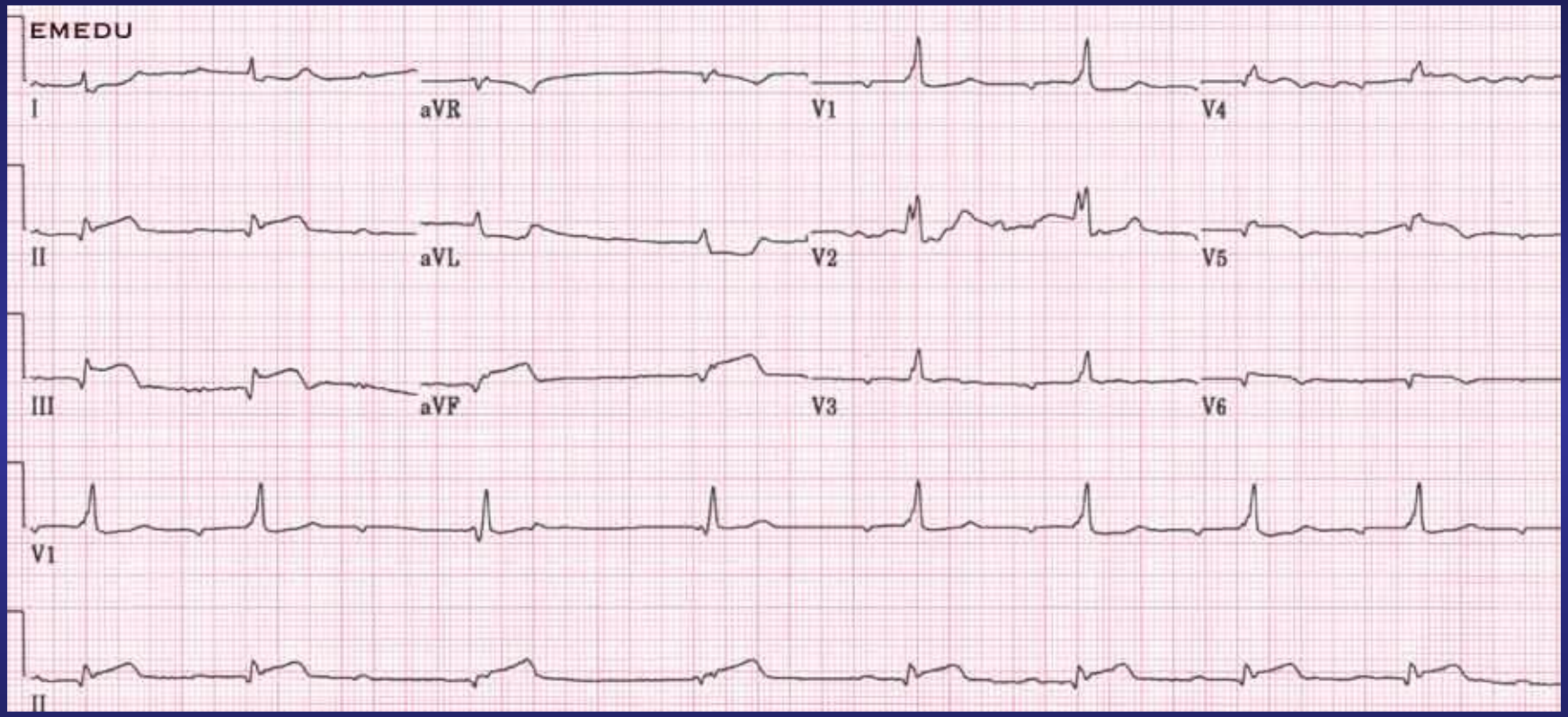

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6

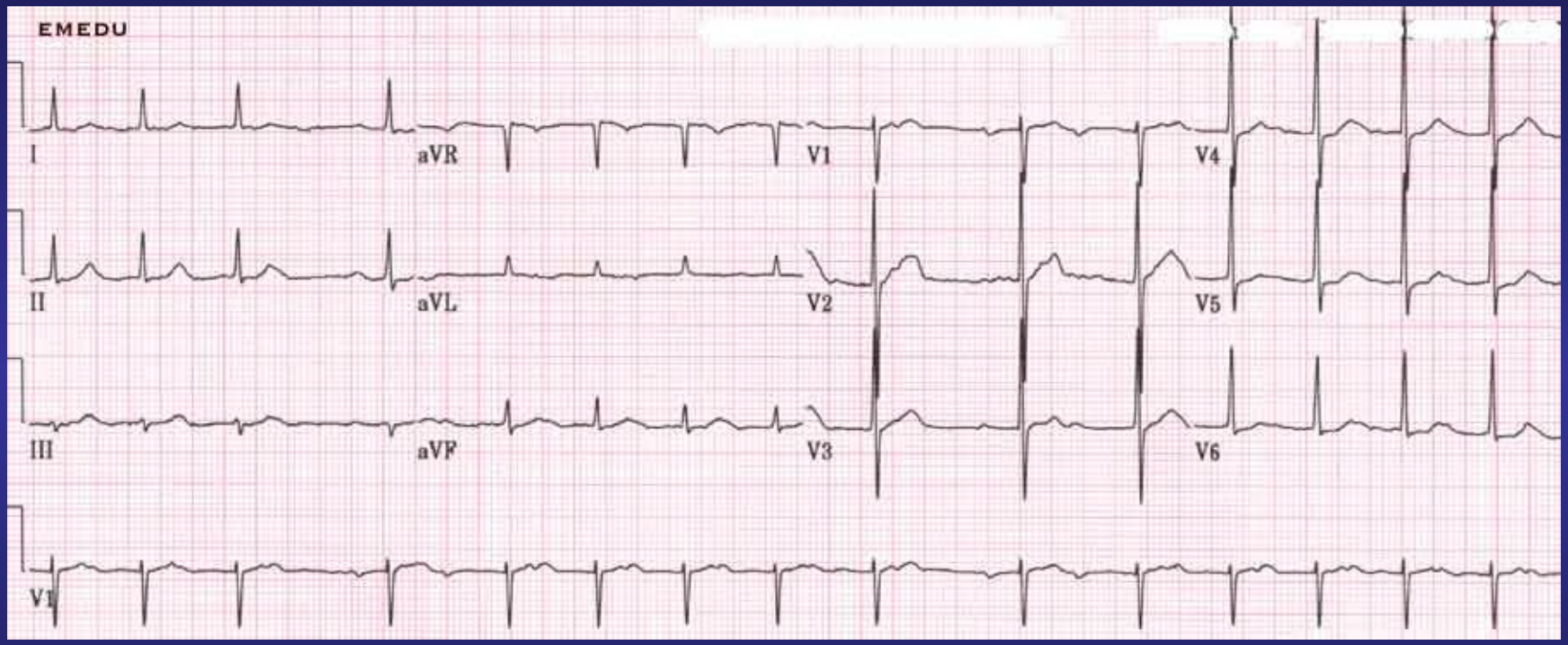

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6

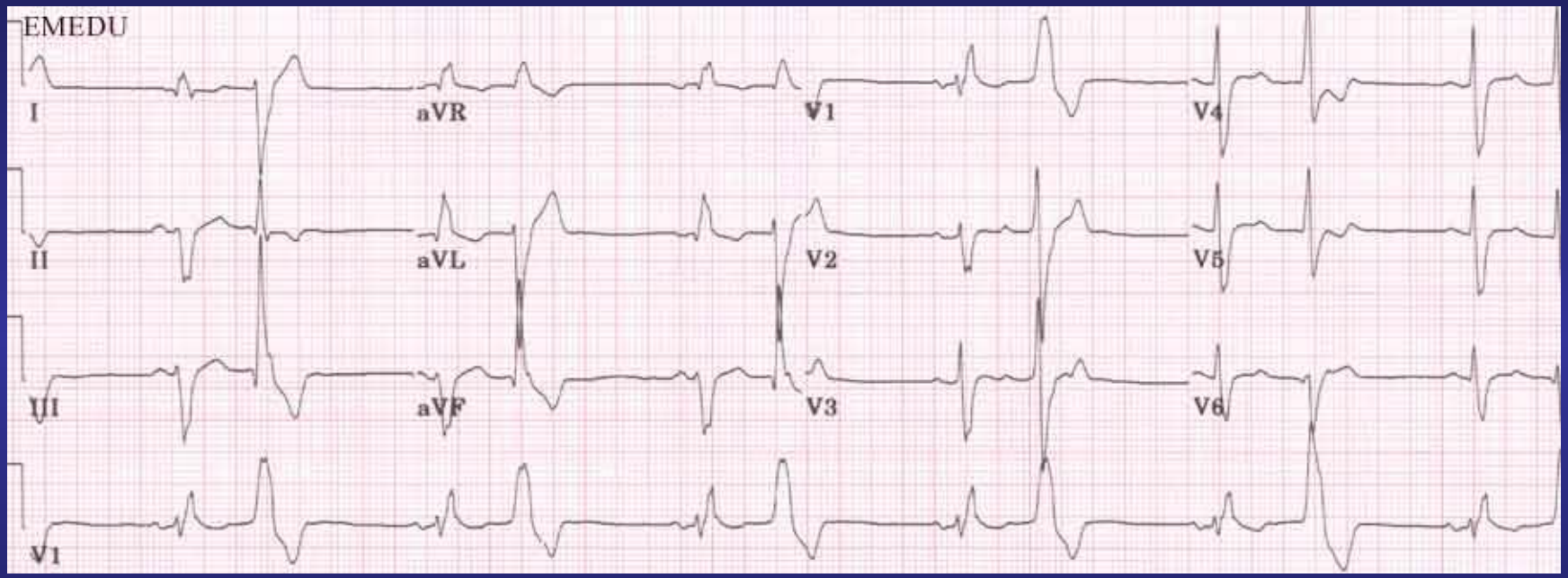

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6
V1
II

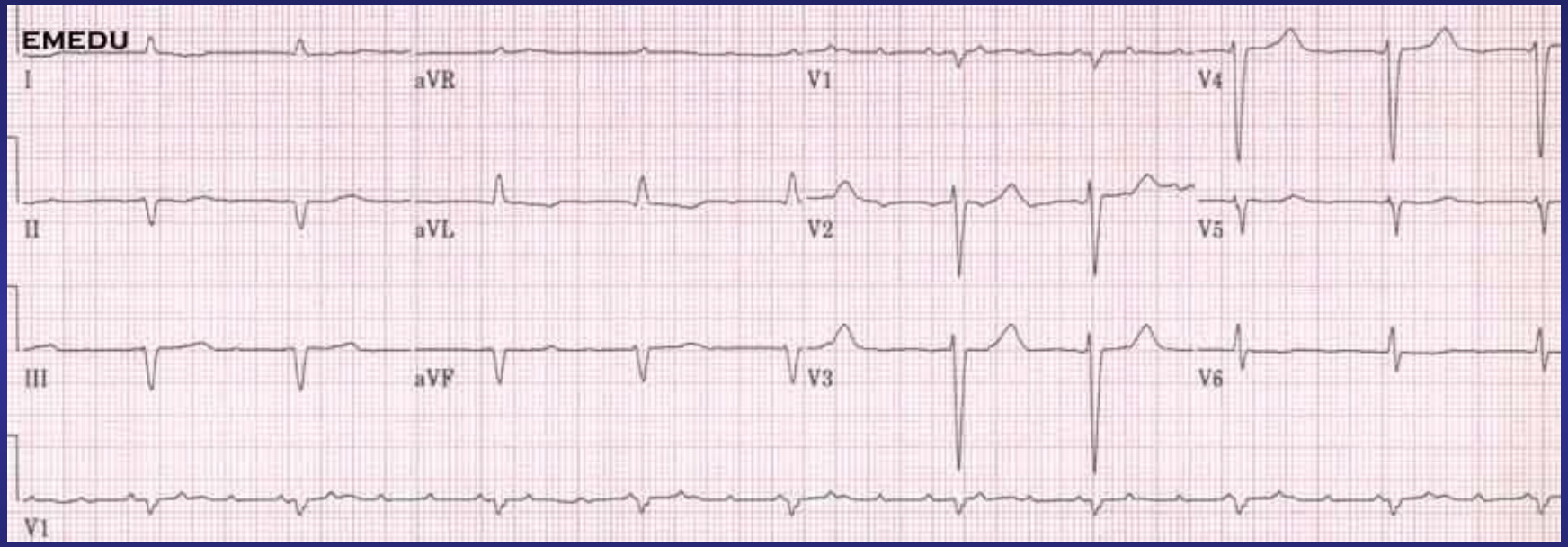

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6
V1

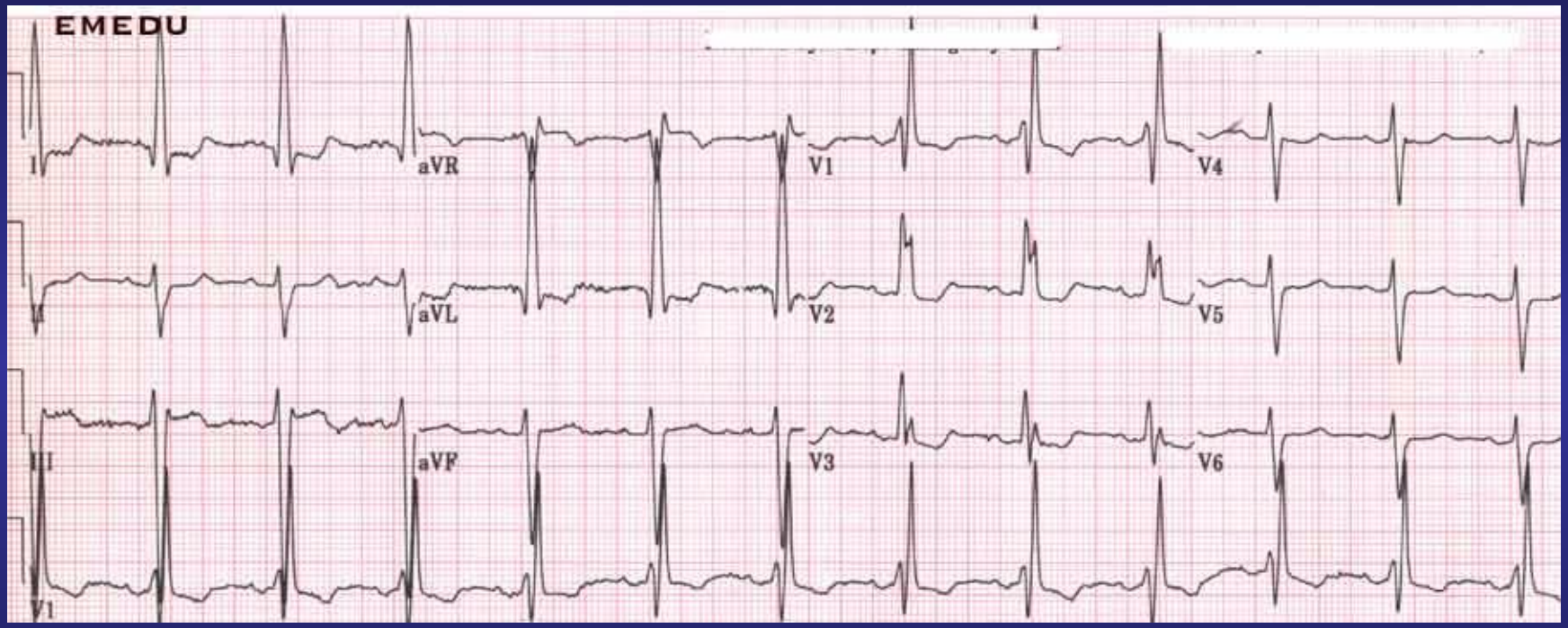

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6
V1

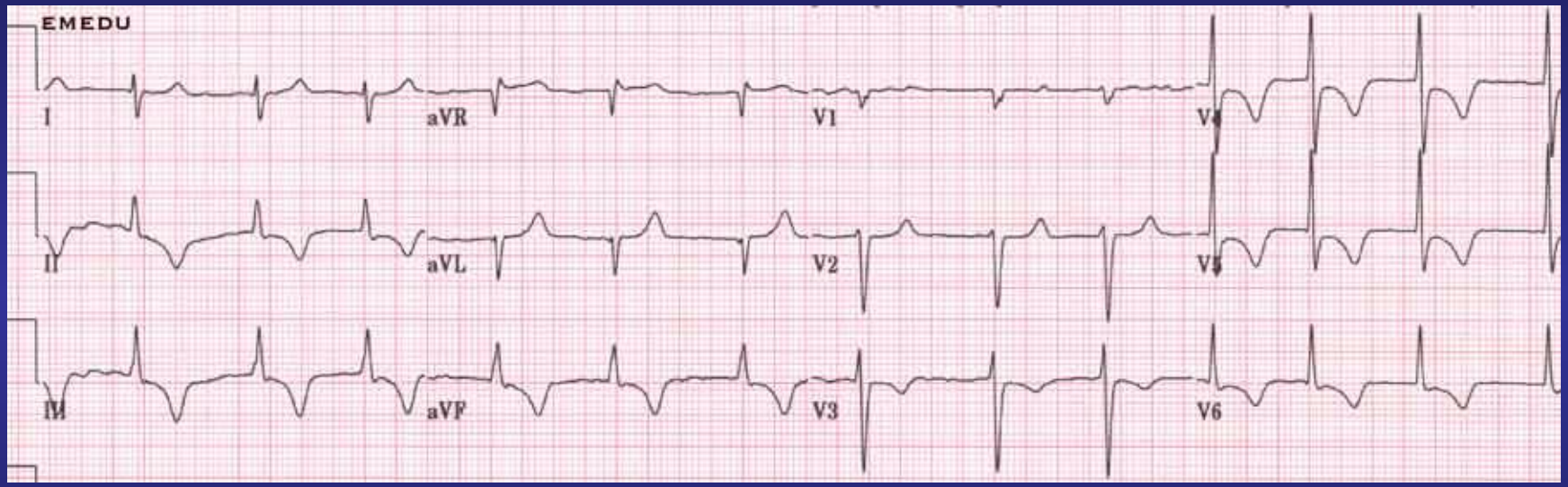

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6
V1
II

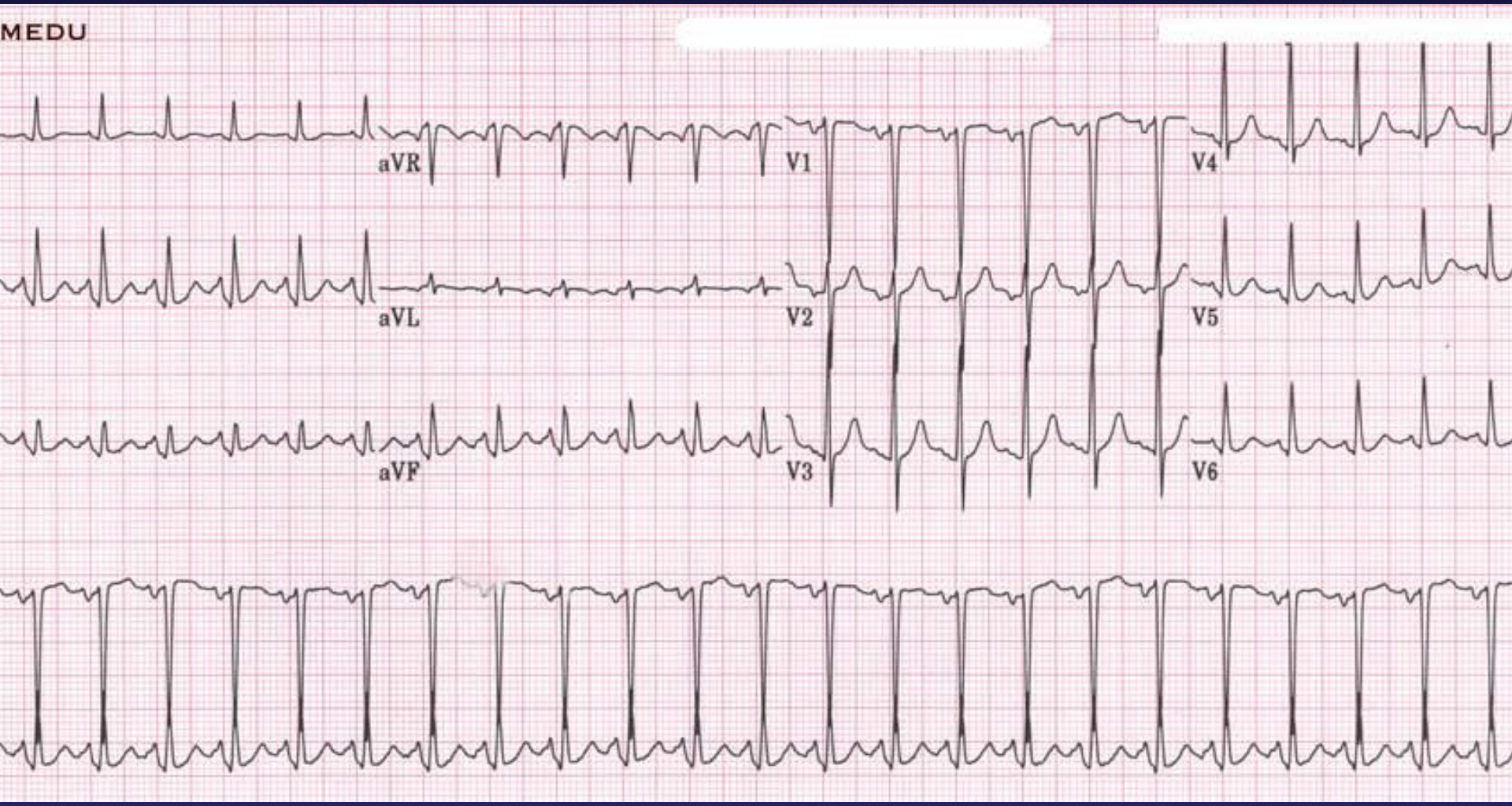

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6
V1

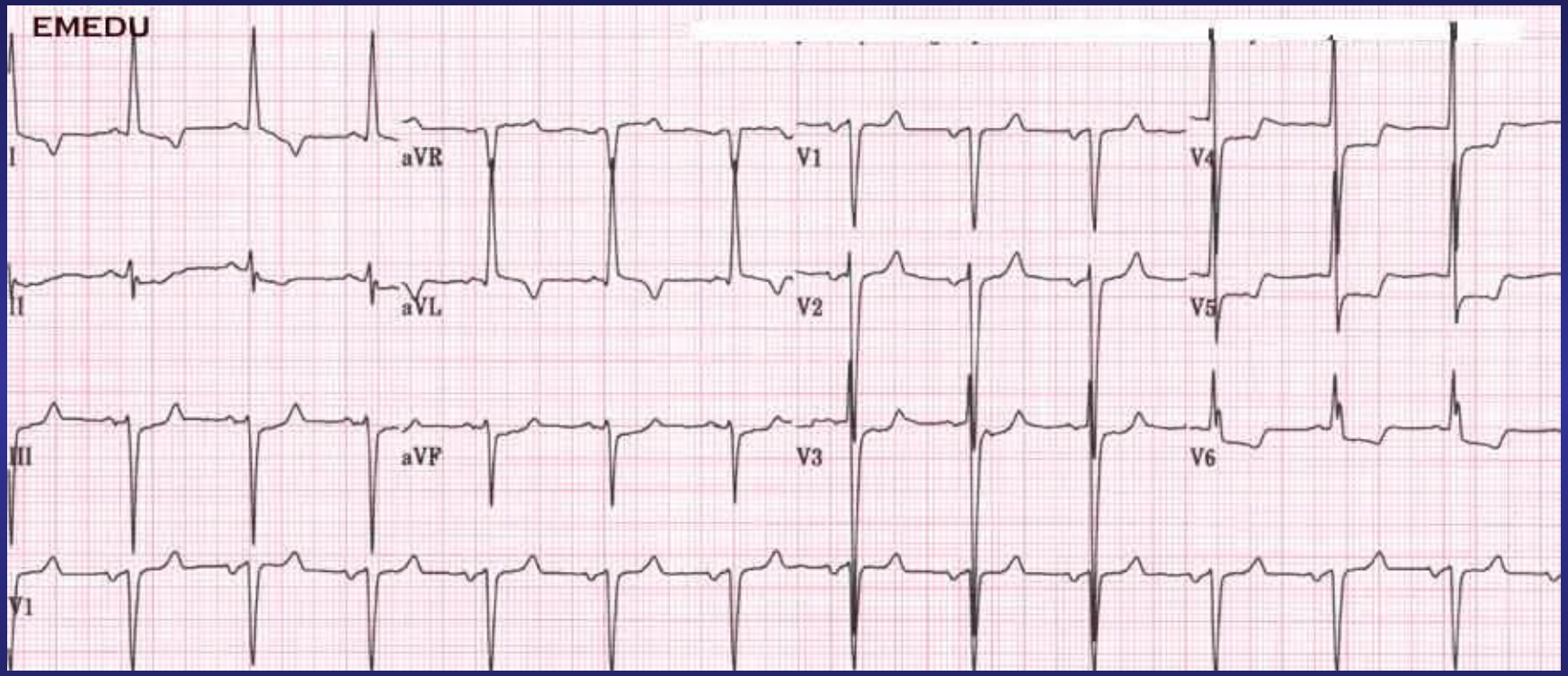

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6
V1

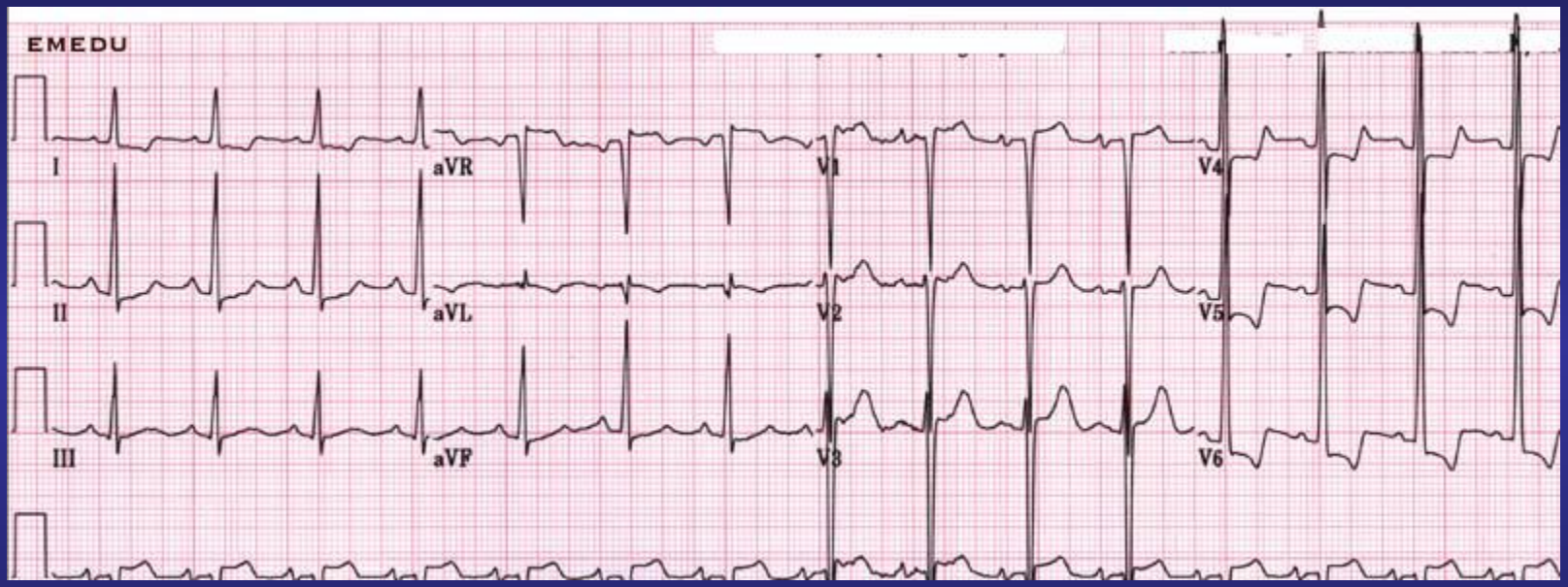

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6
V1

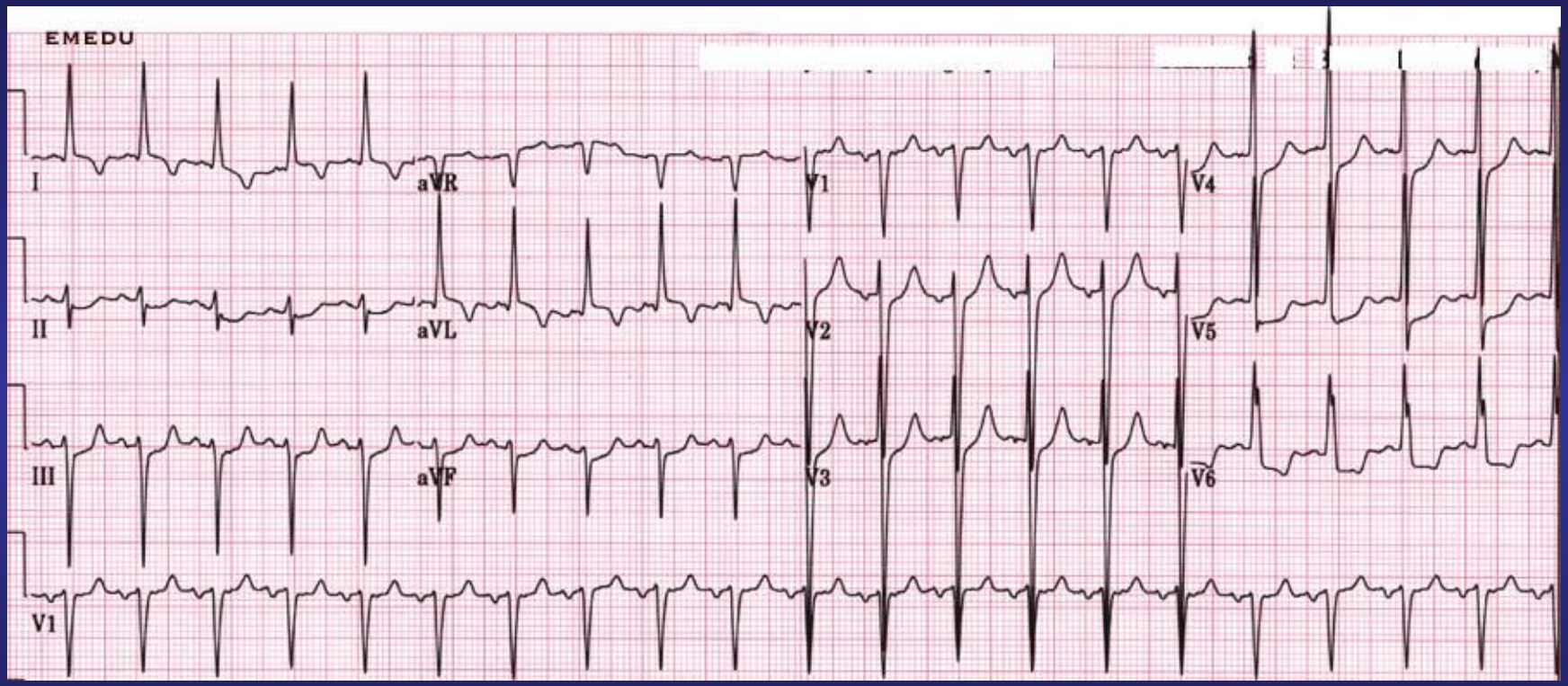

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6
V1

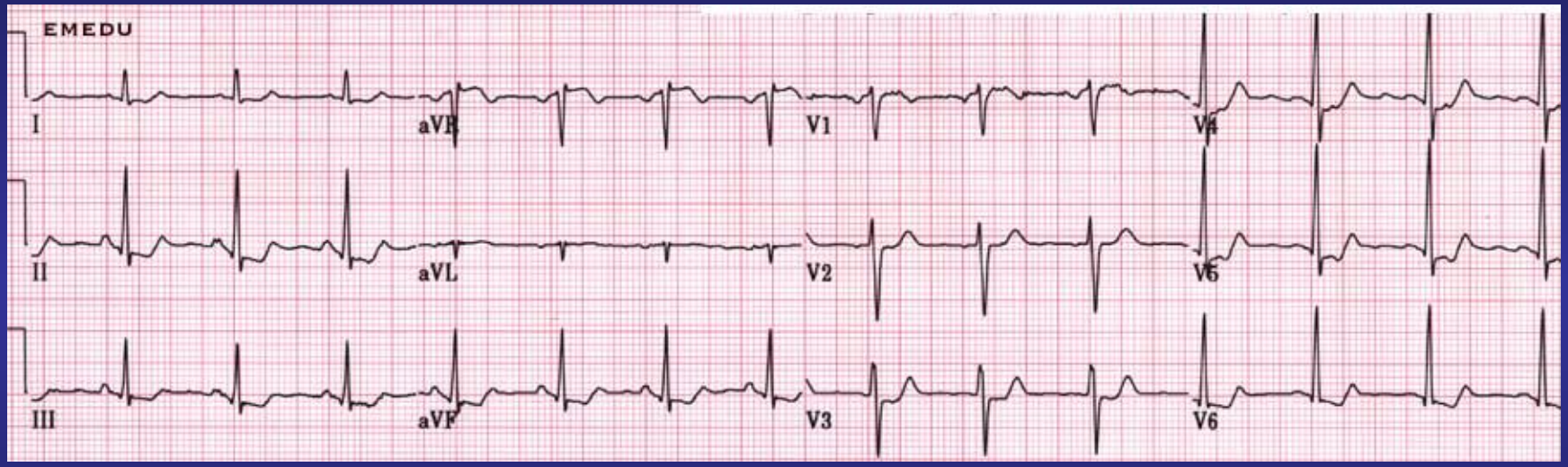

EMEDU
I
aVR
V1
II
aVL
V2
III
aVF
V3
V6

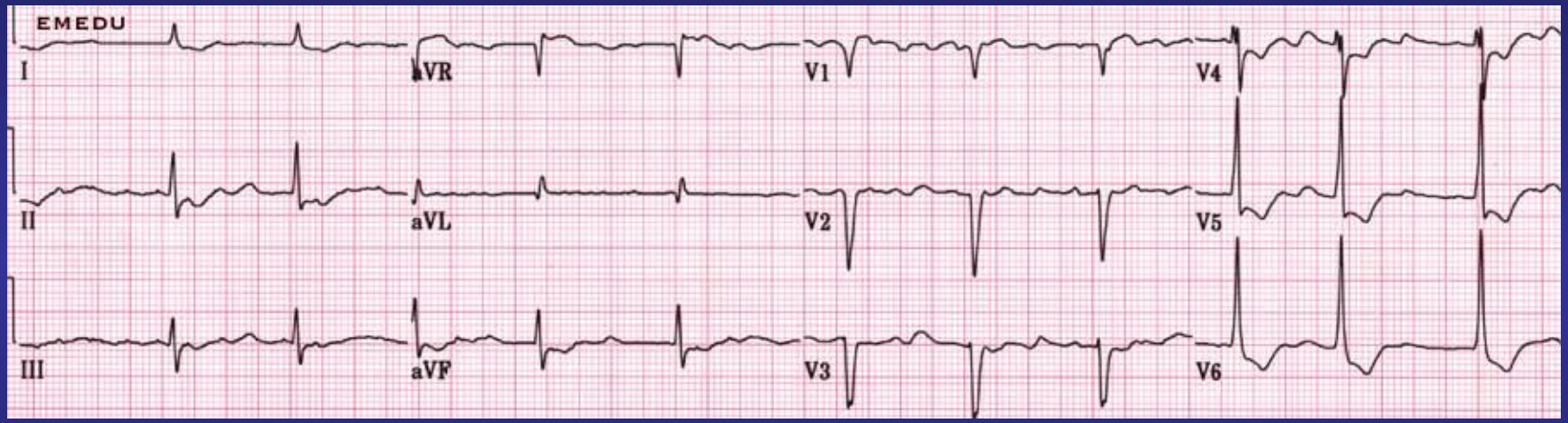

MEDU
aVR
V1
V4
aVL
V2
V5
aVF
V3
V6

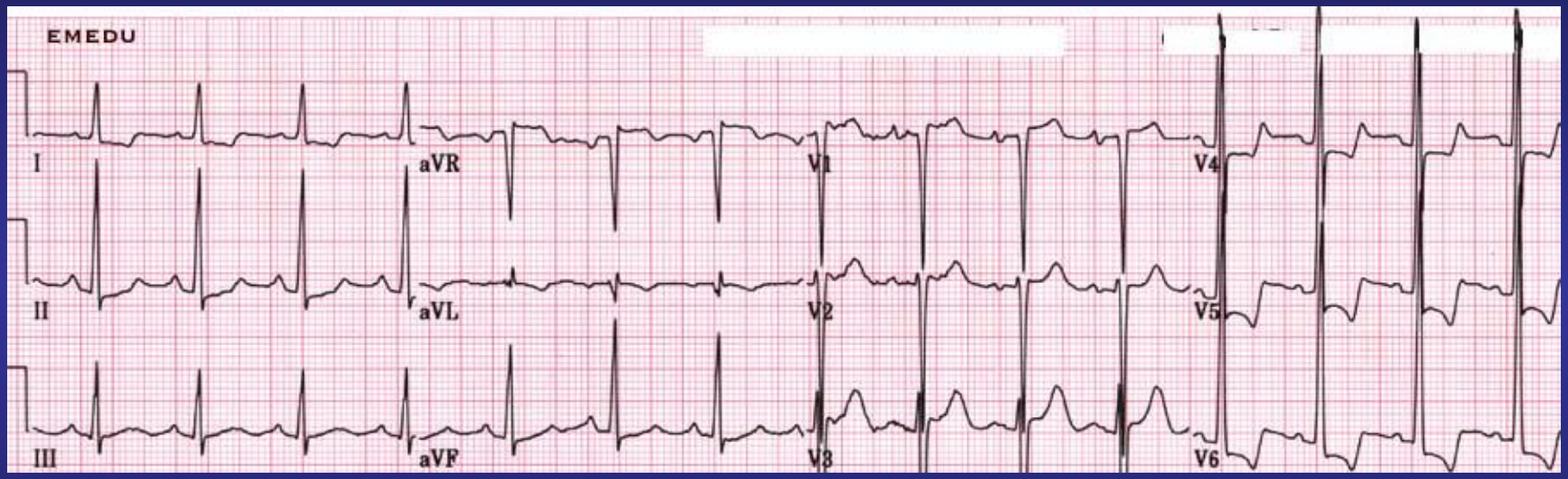

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6
V1

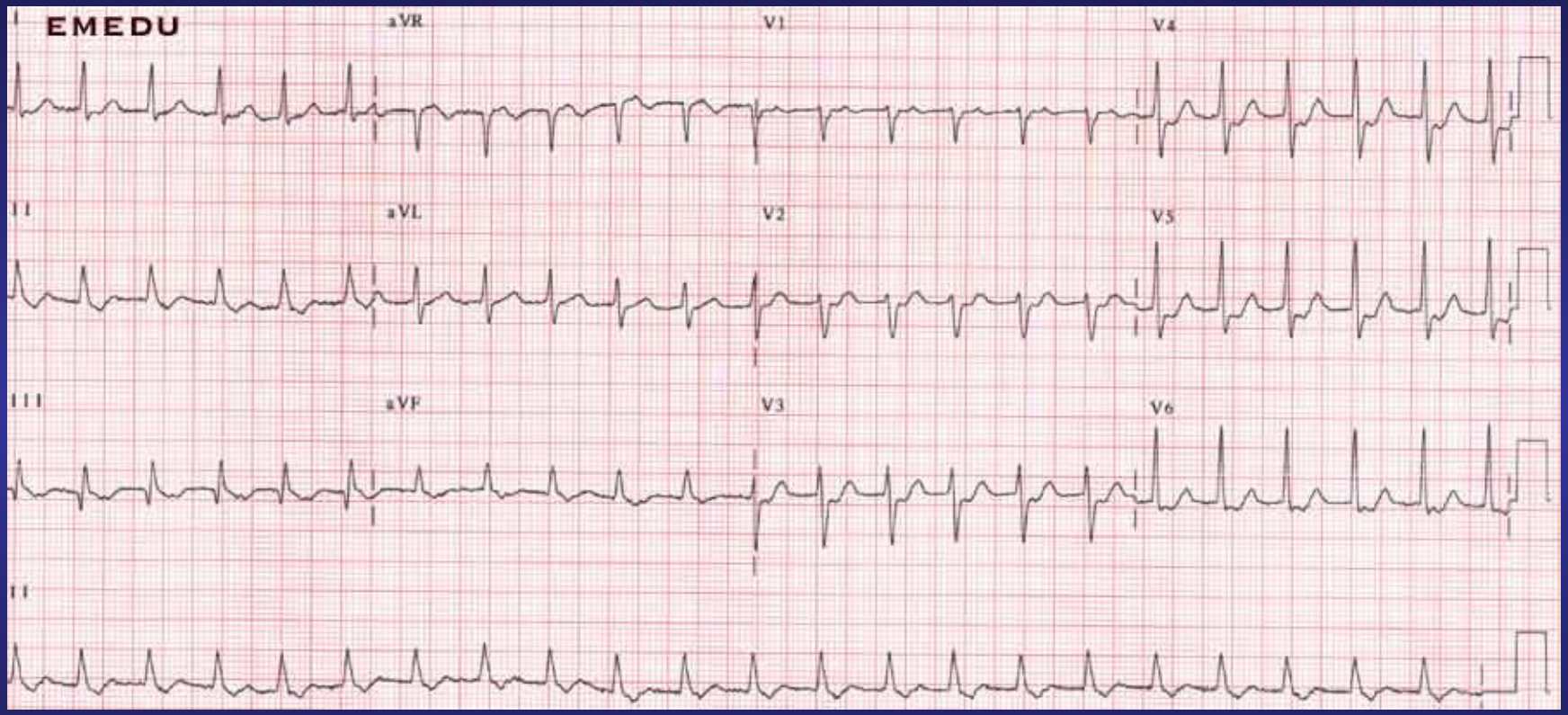

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6

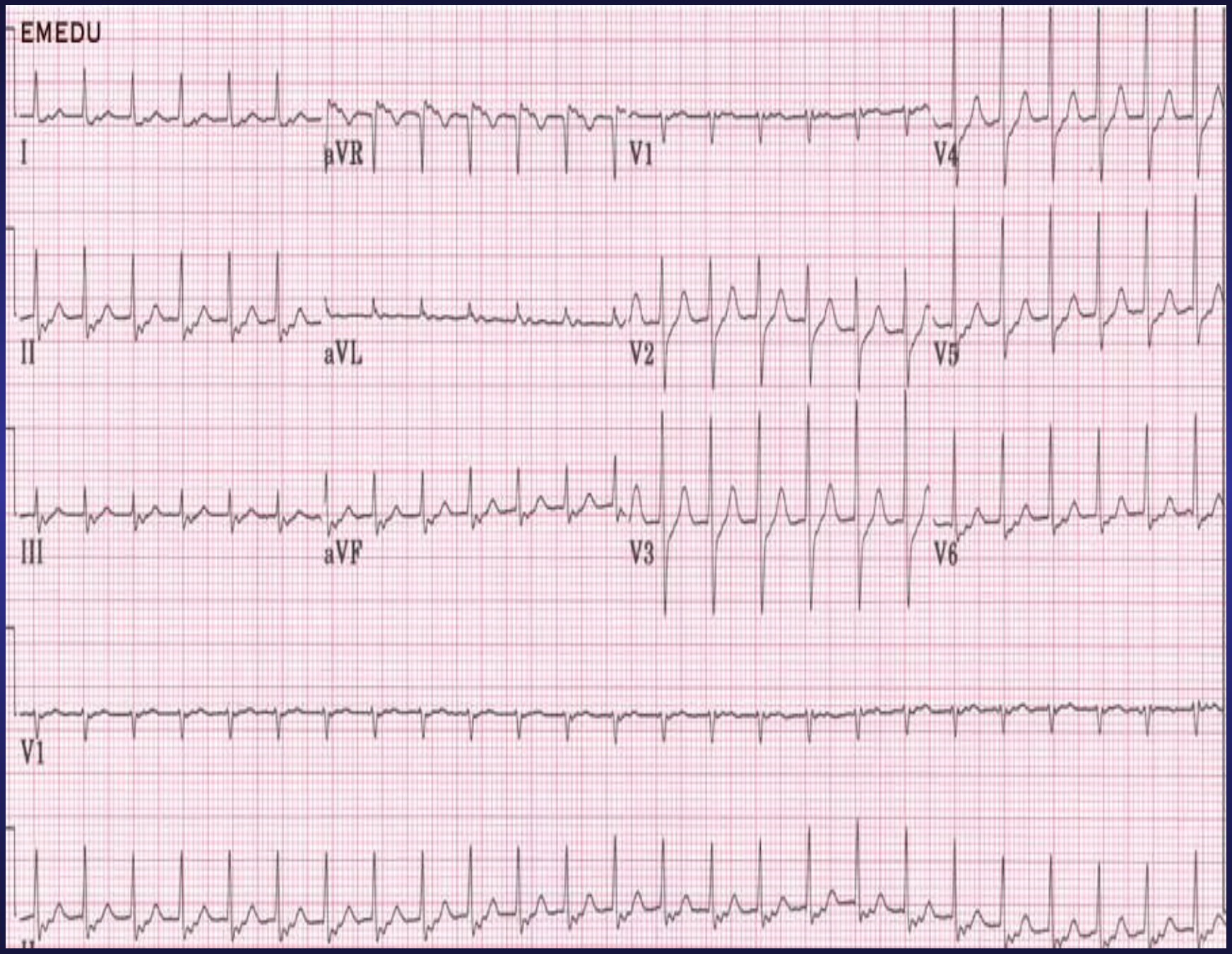

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6
V1

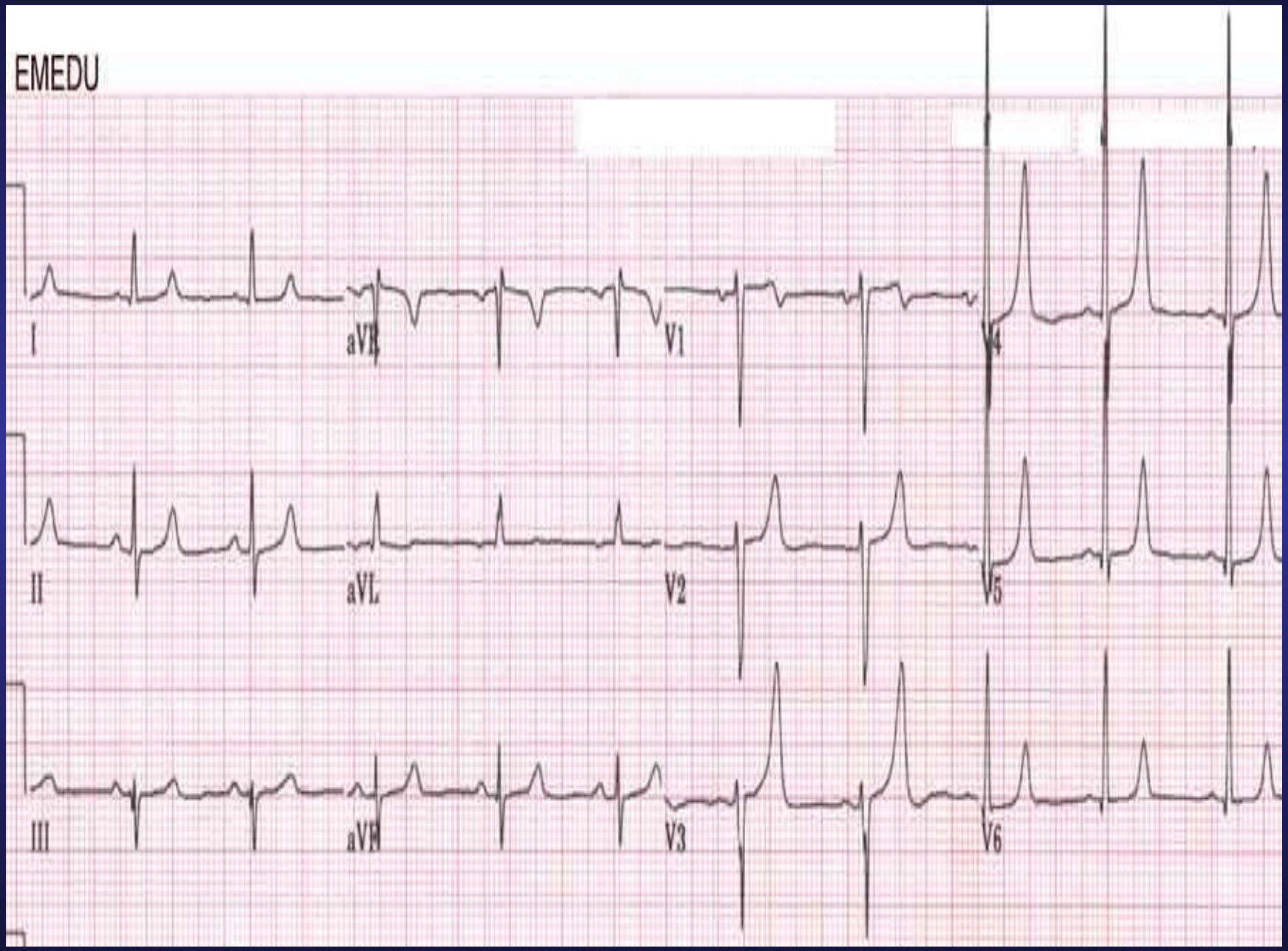

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6

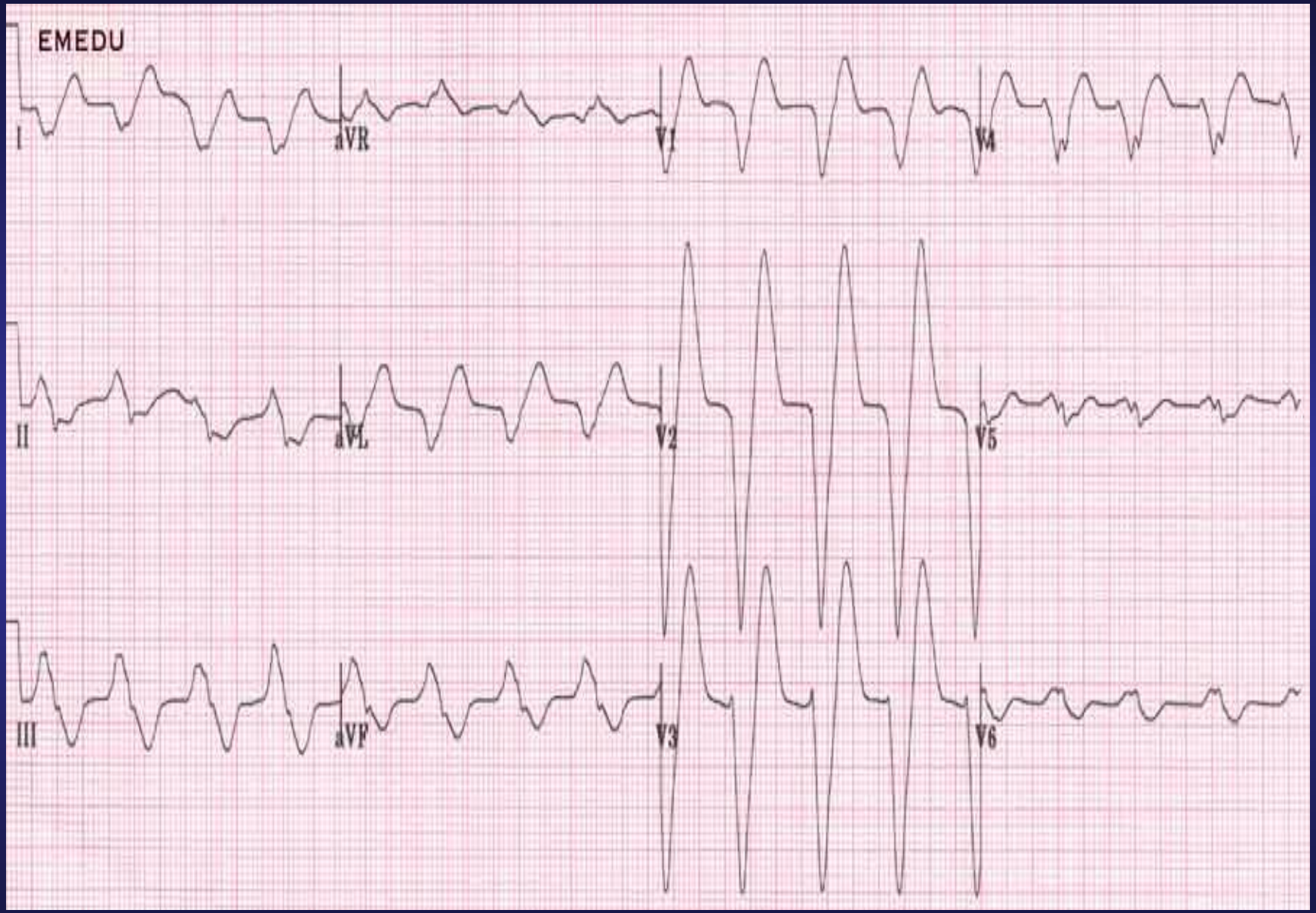

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6

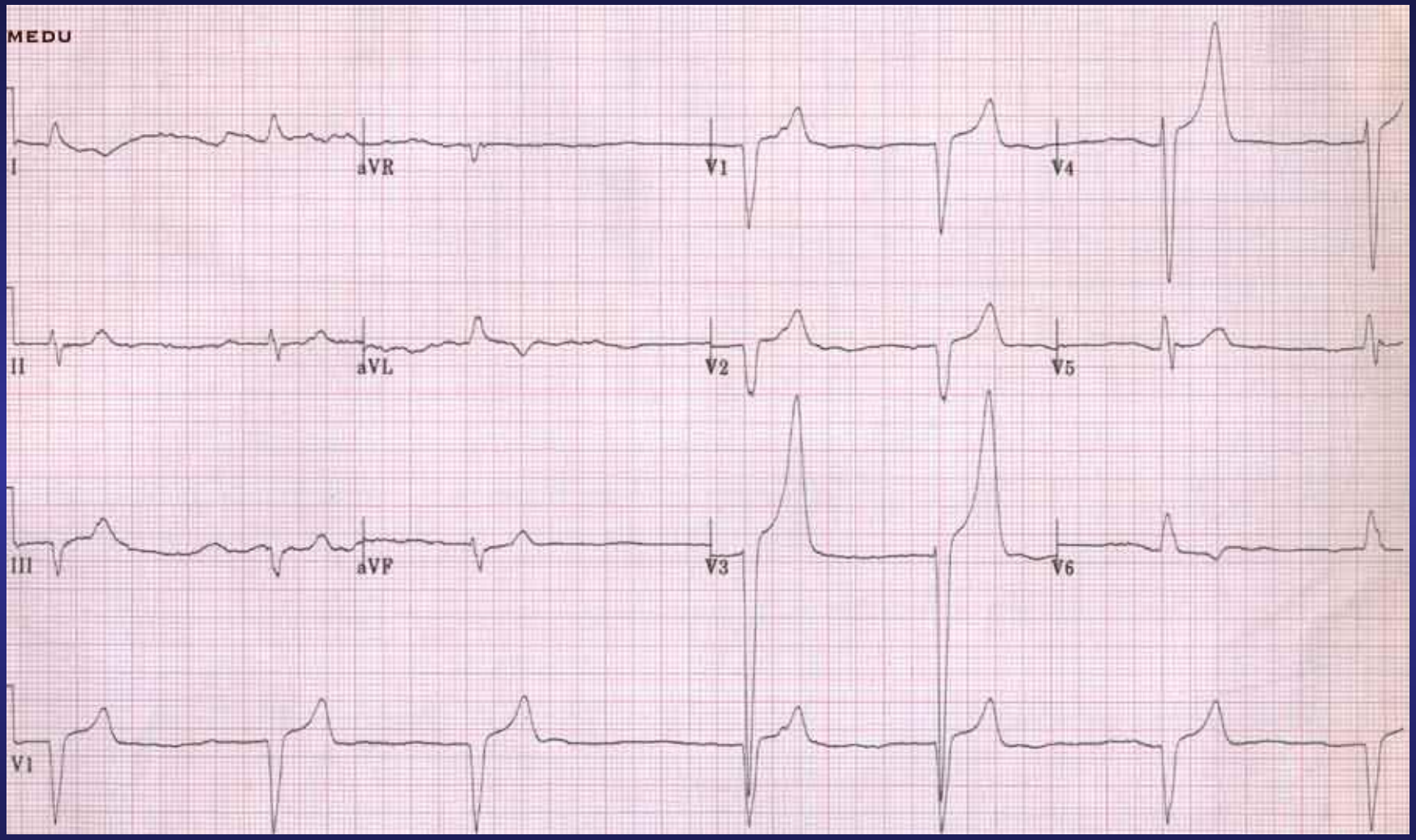

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6

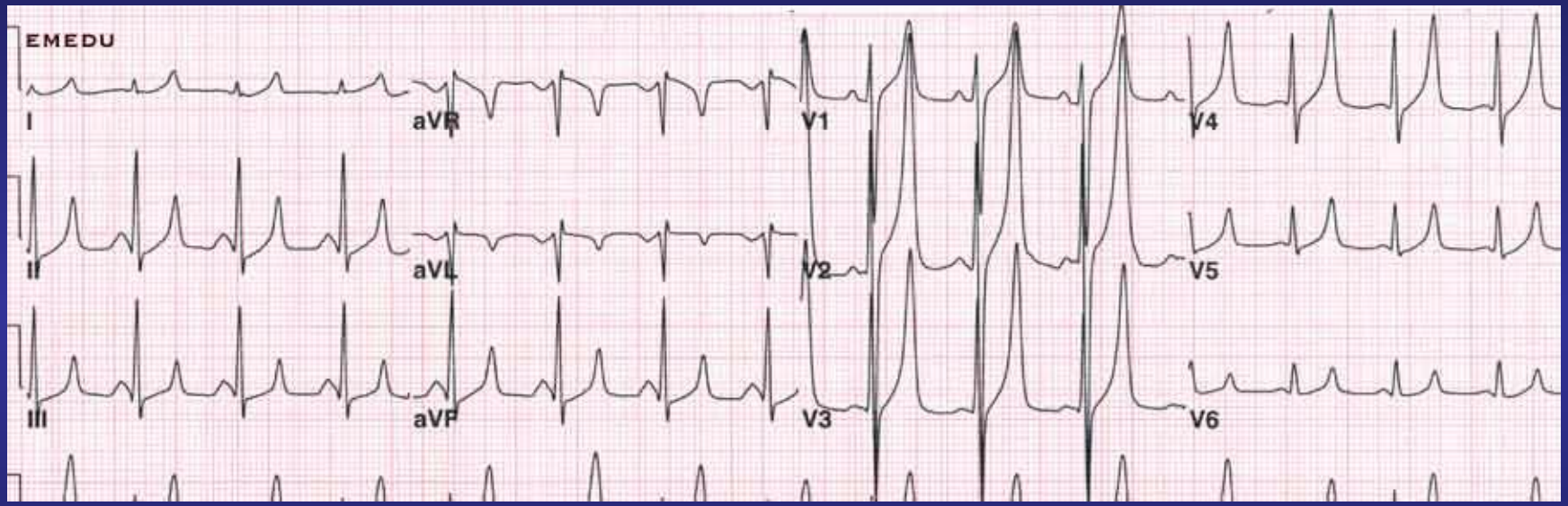

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6
II

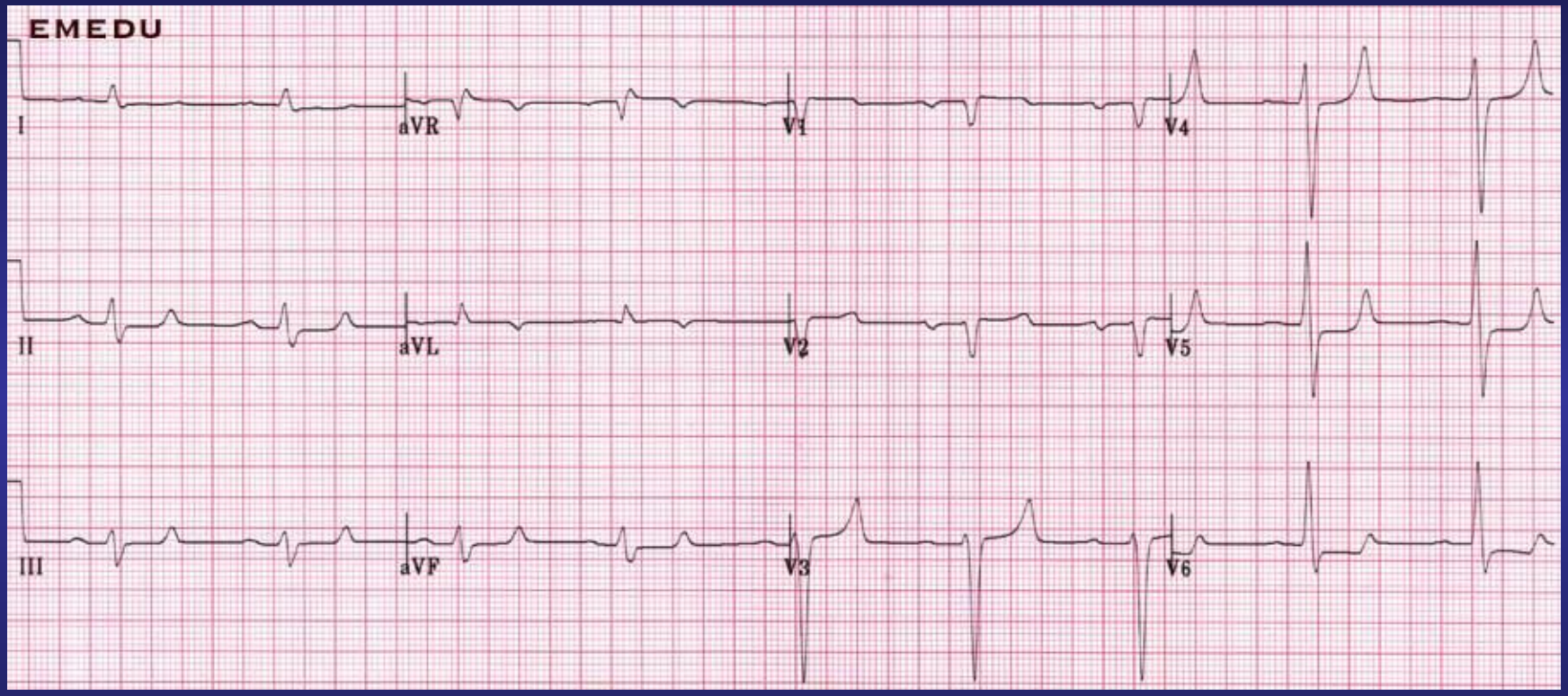

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6
V1

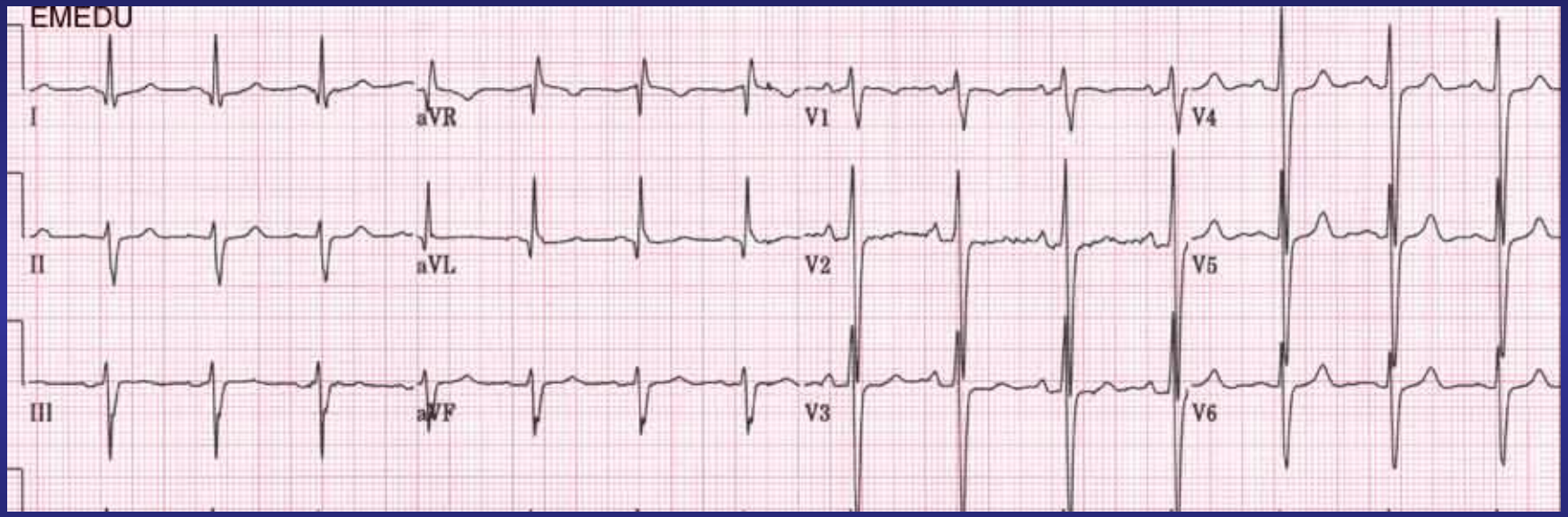

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6

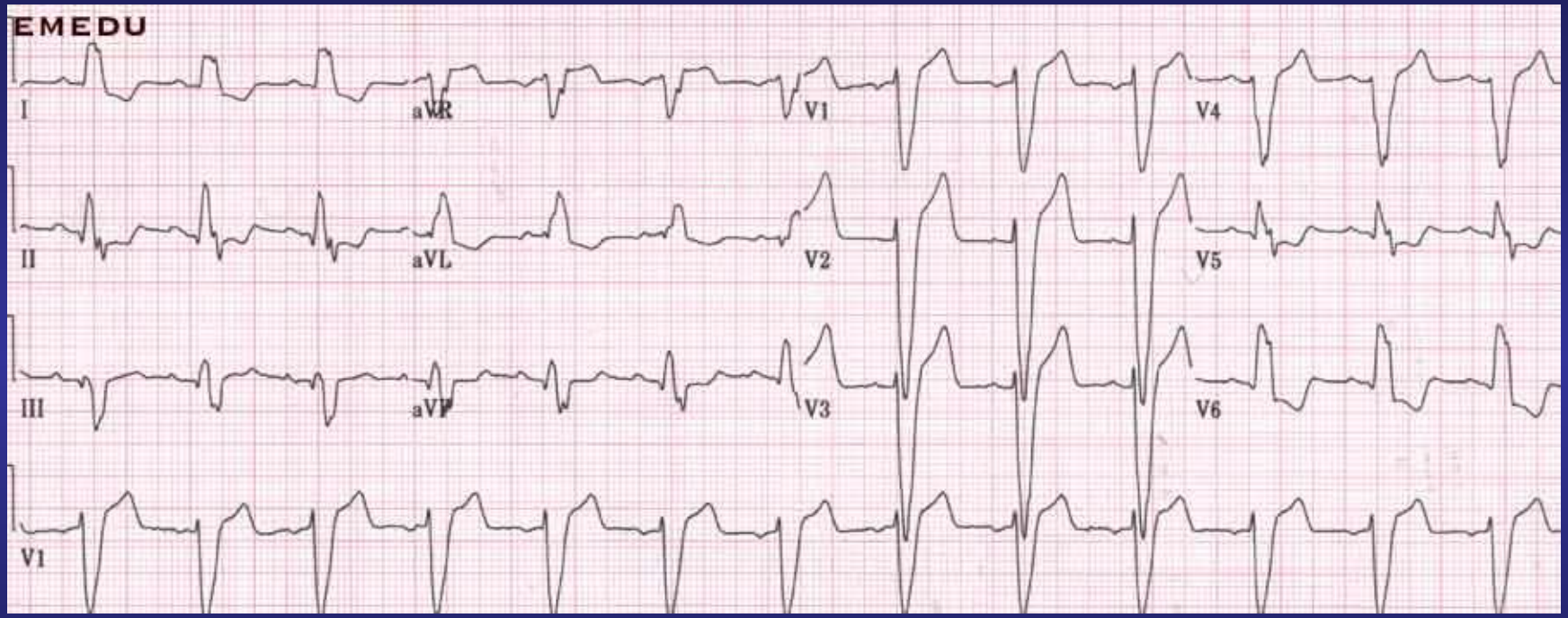

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6

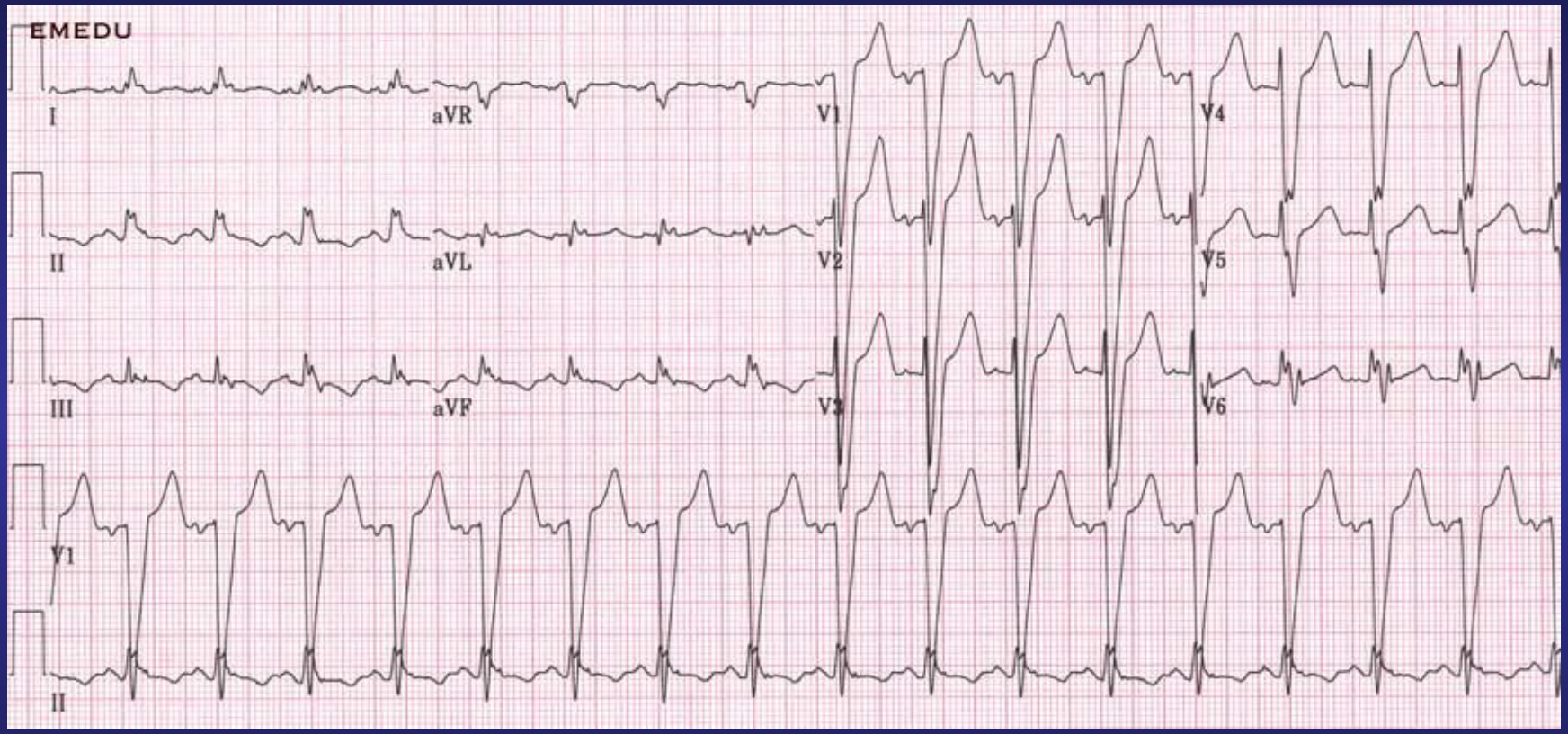

MEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6
V1

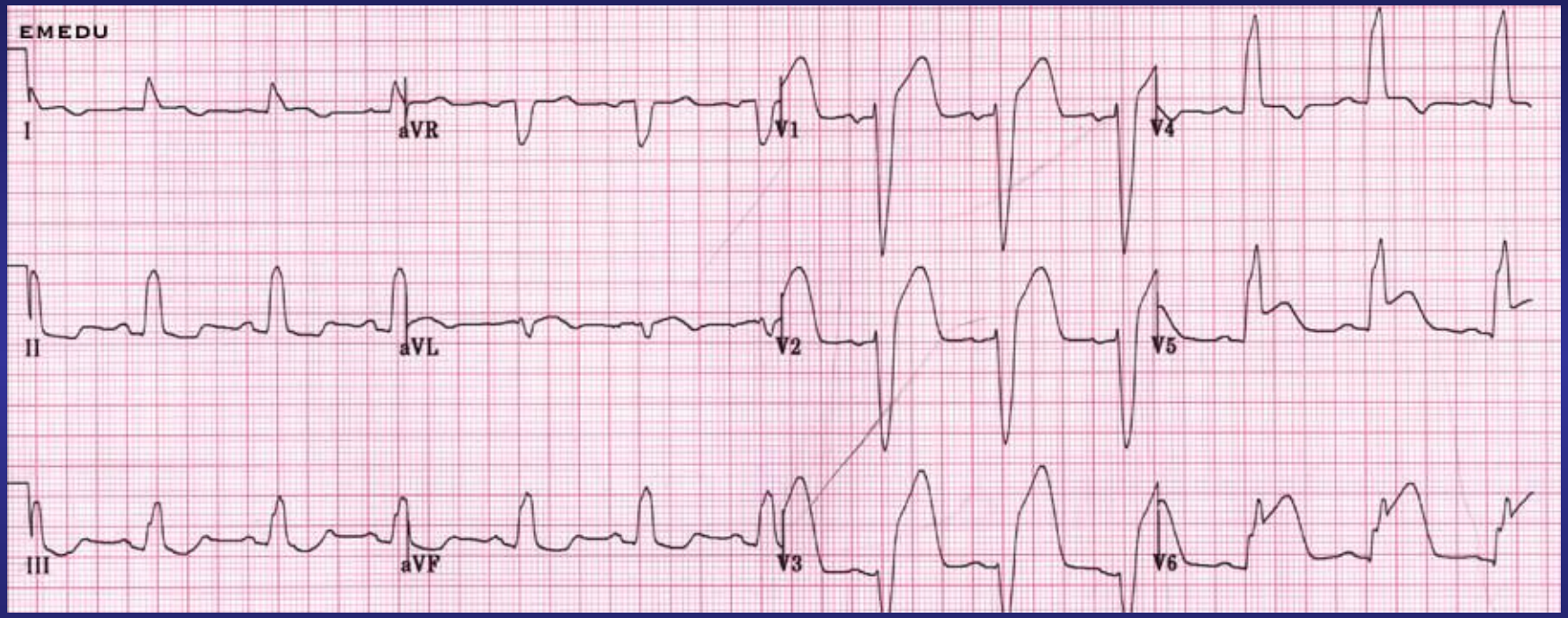

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6

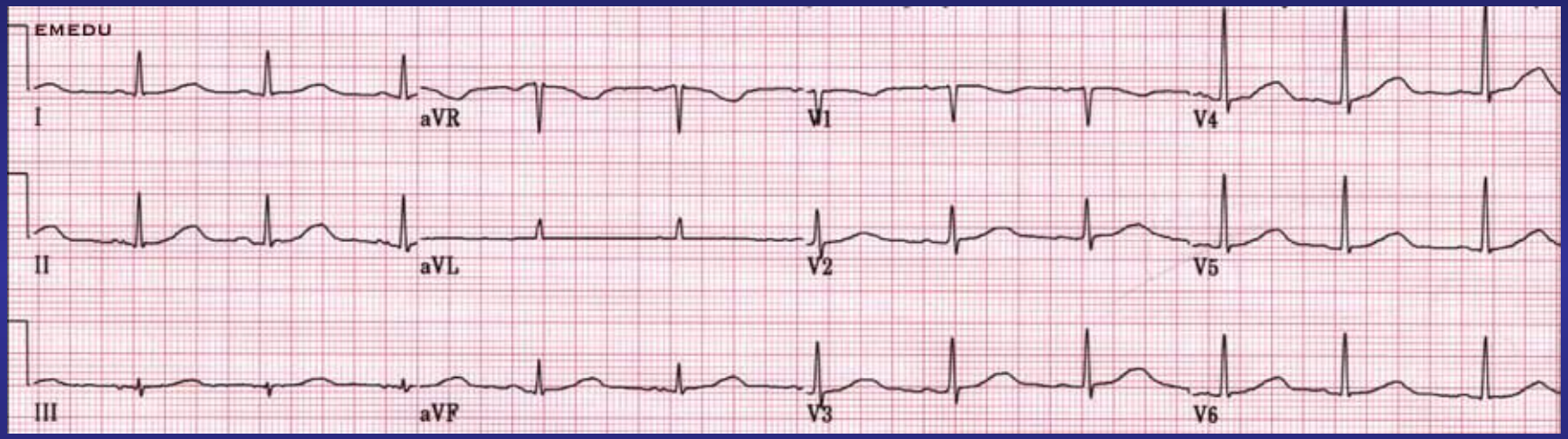

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6

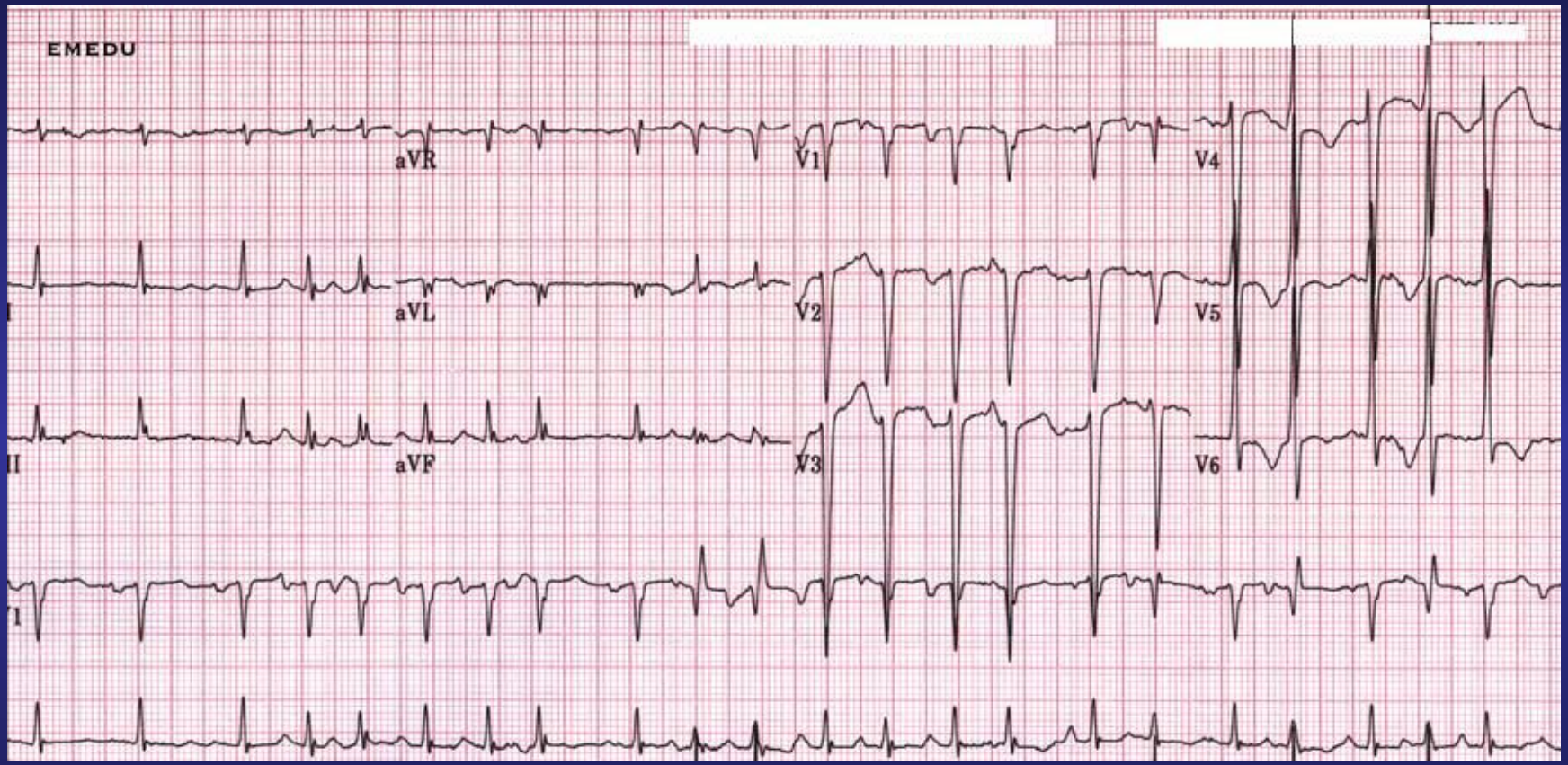

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6

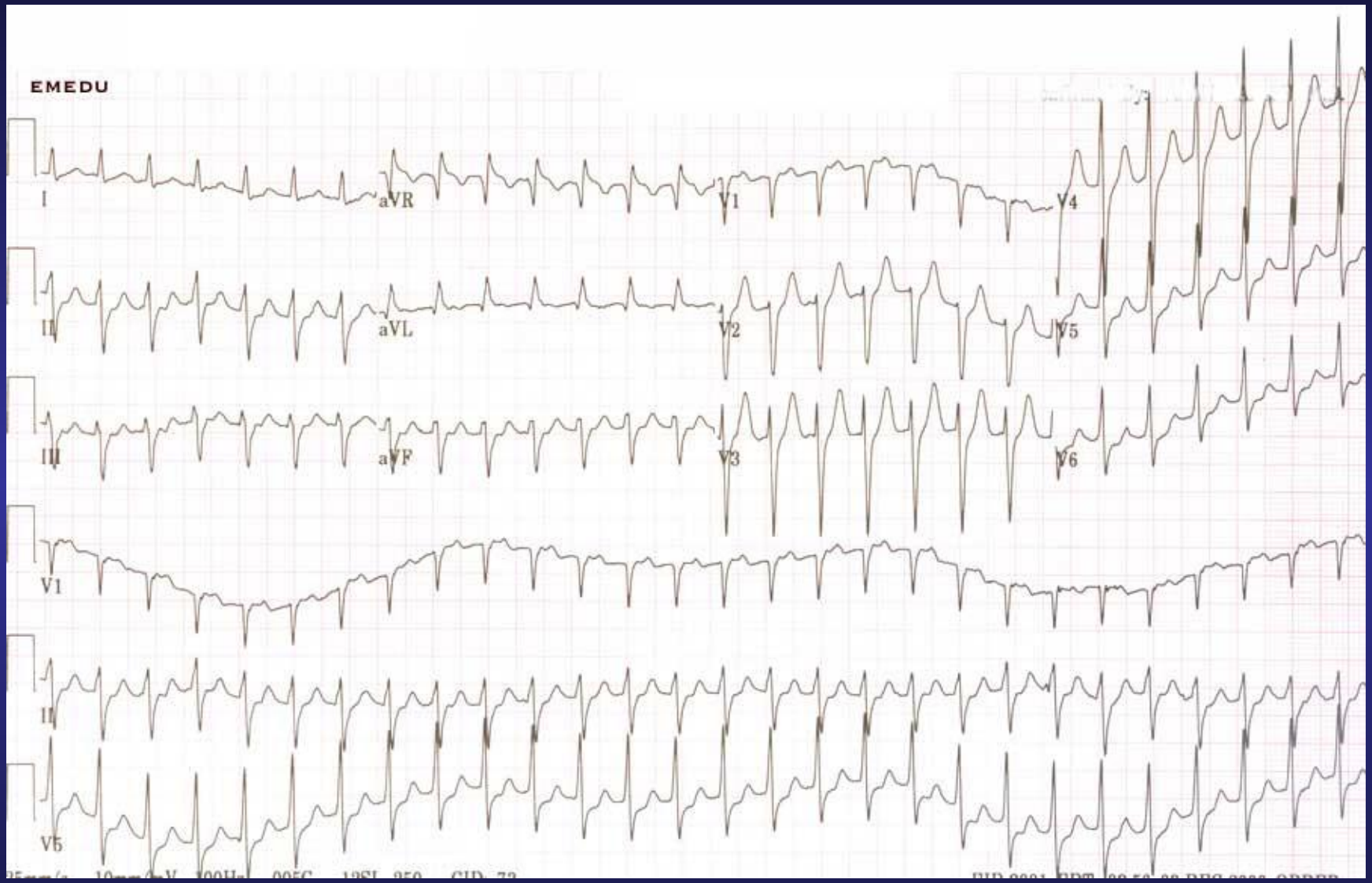

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6
V1

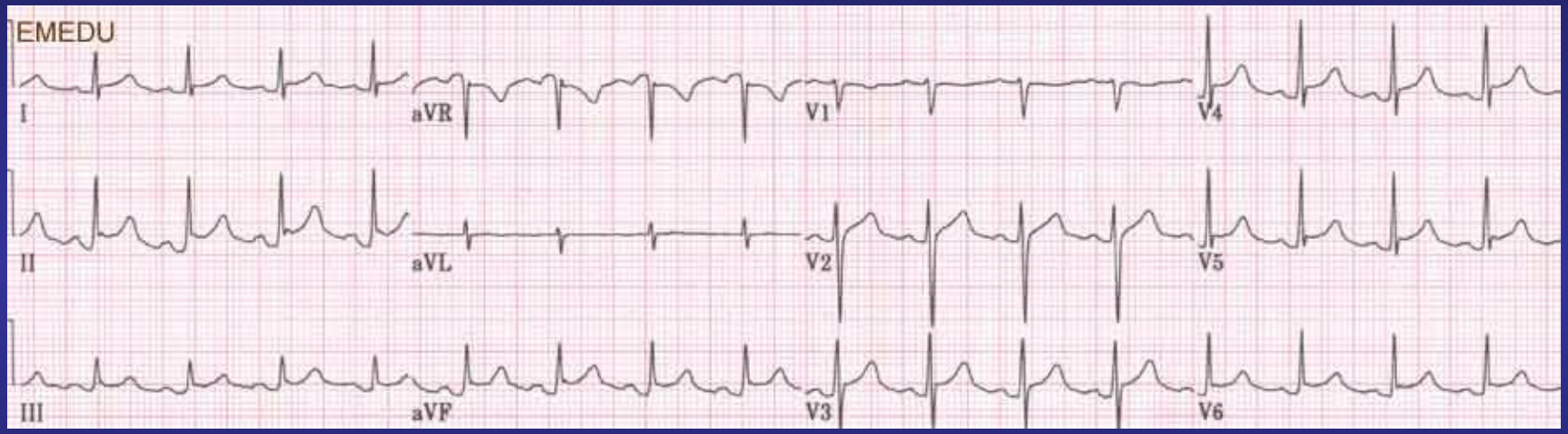

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6
V1
II

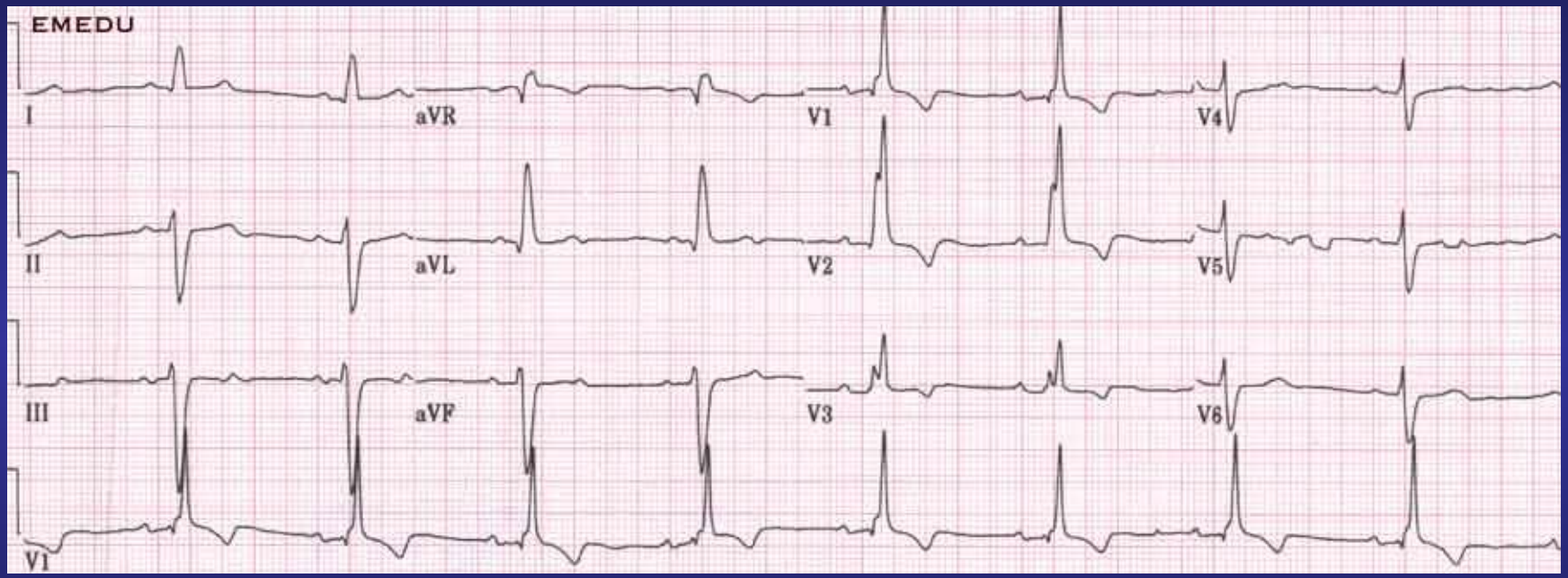

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6

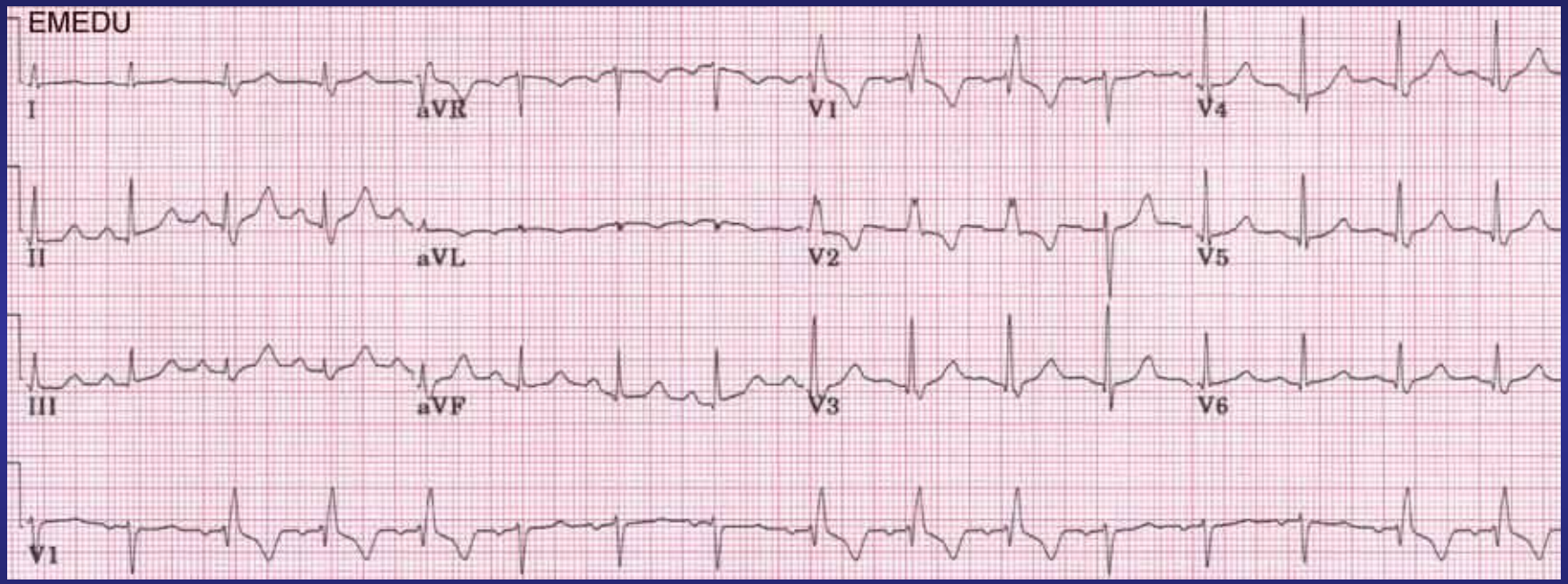

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6

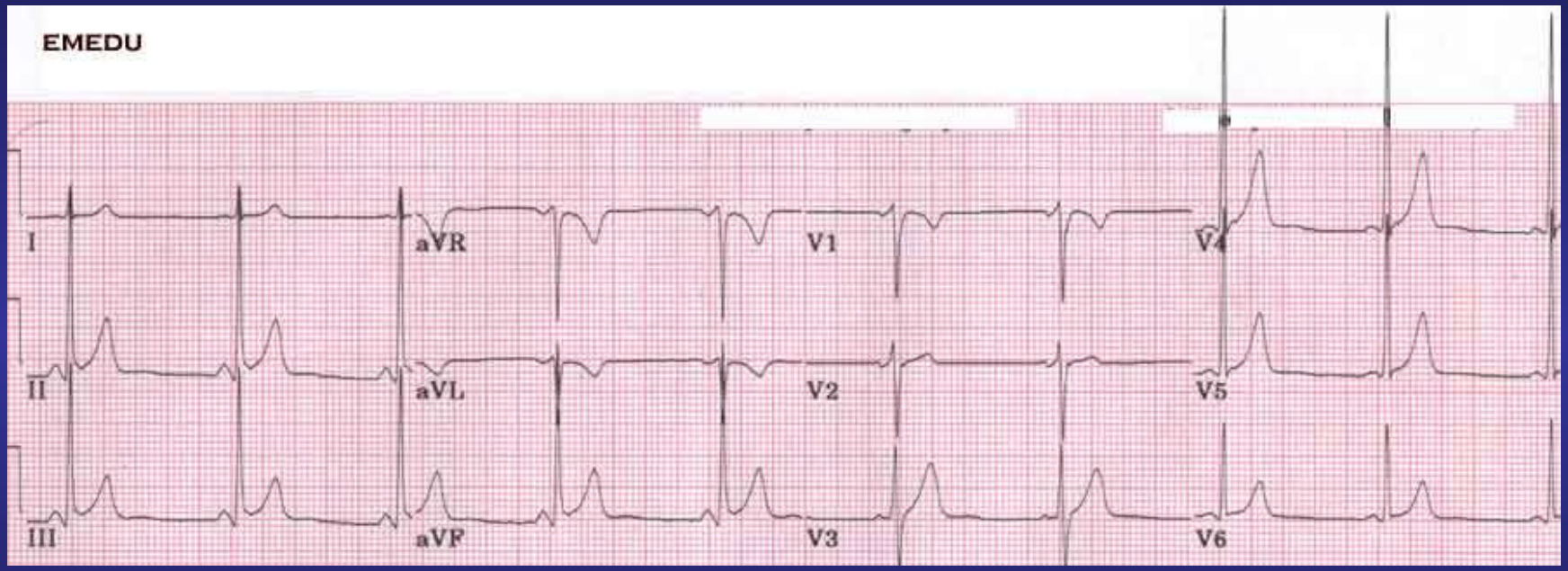

EMEDU
aVR
V1
V4
aVL
V2
V5
aVF
V3
V6

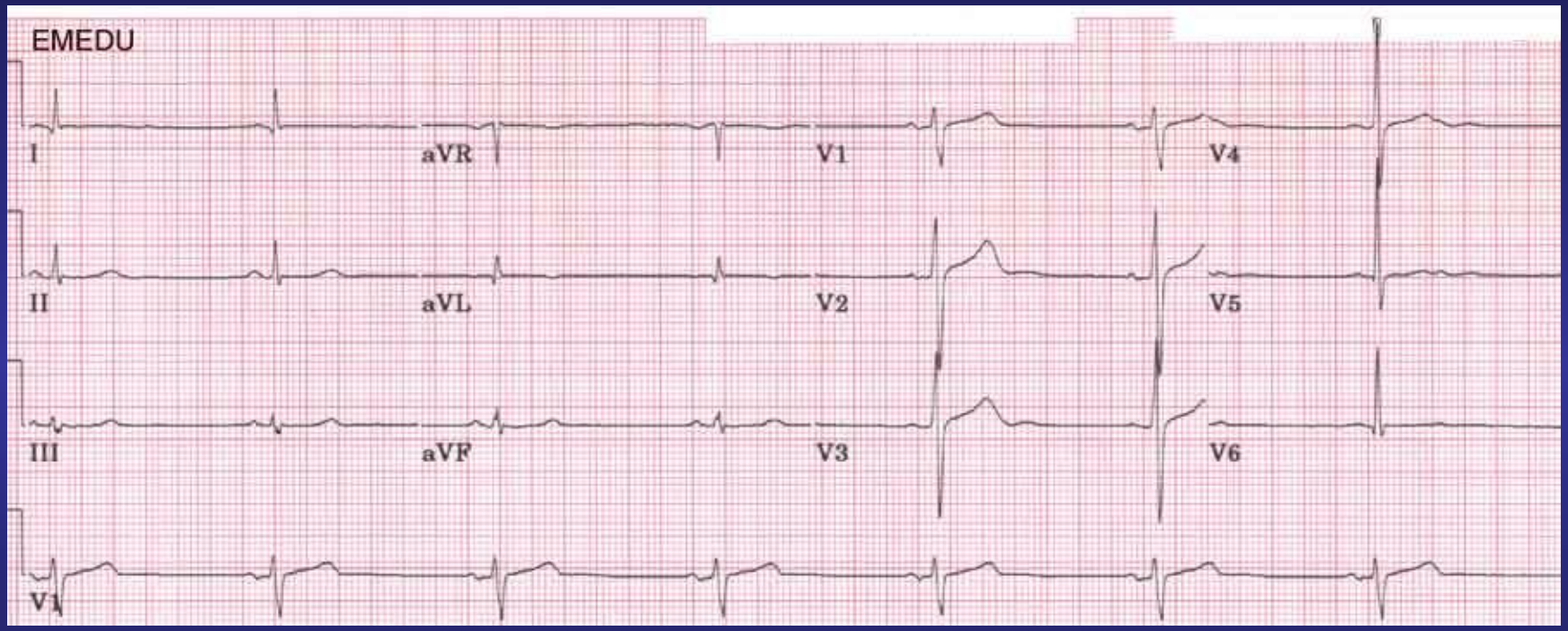

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6
V1
II
V5

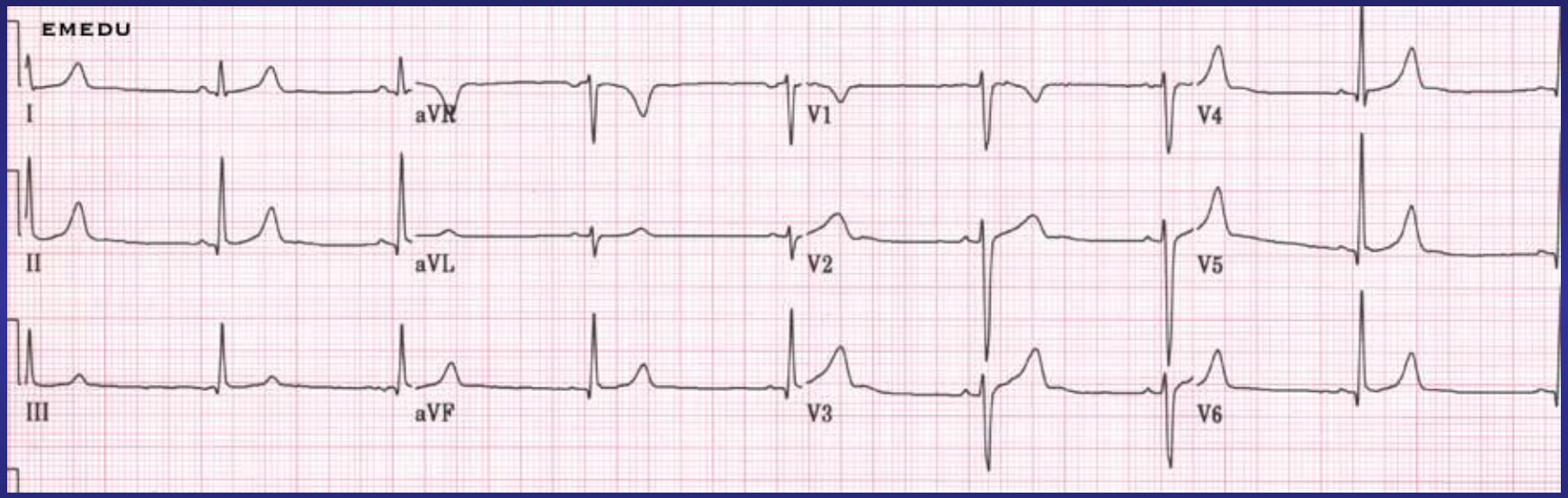

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6

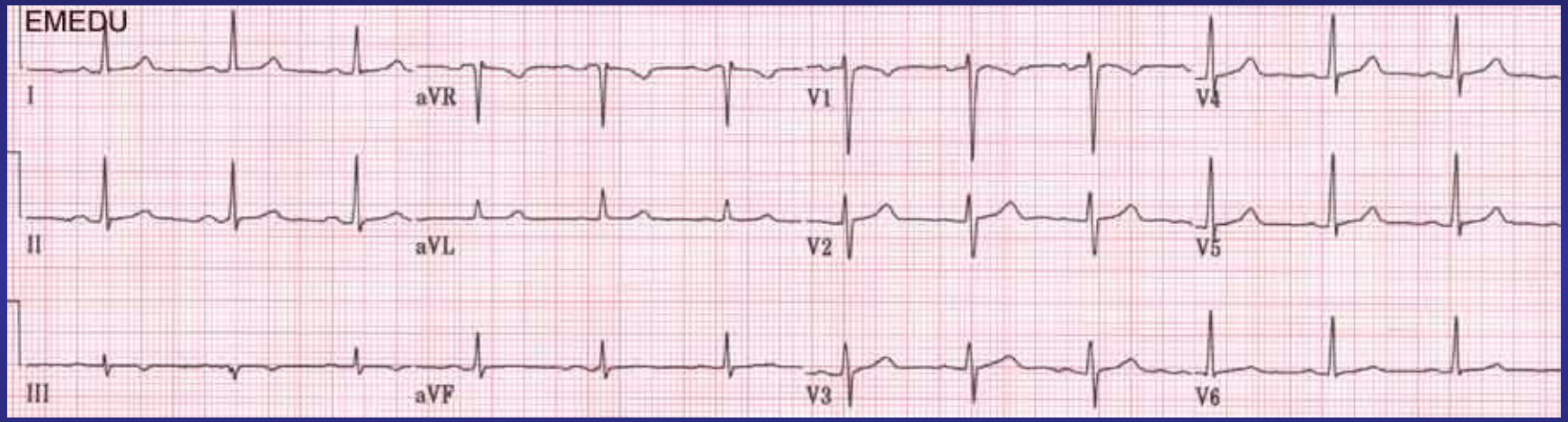

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6
V1

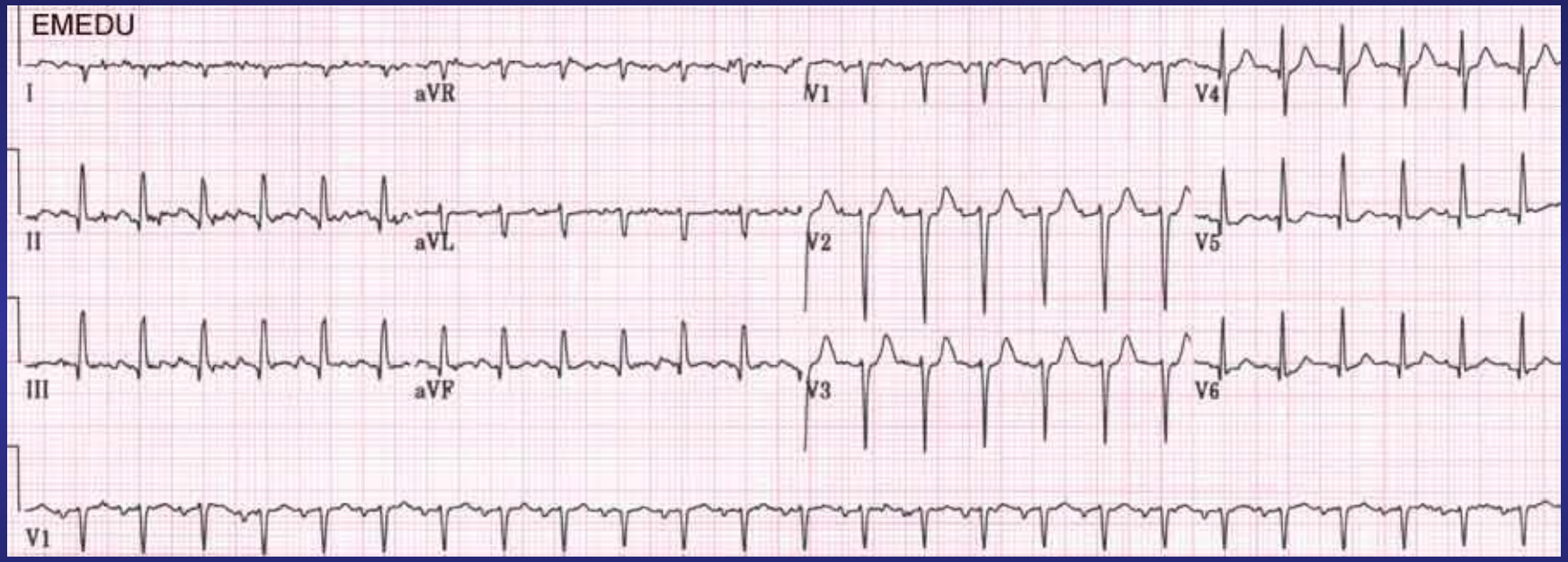

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6
V1

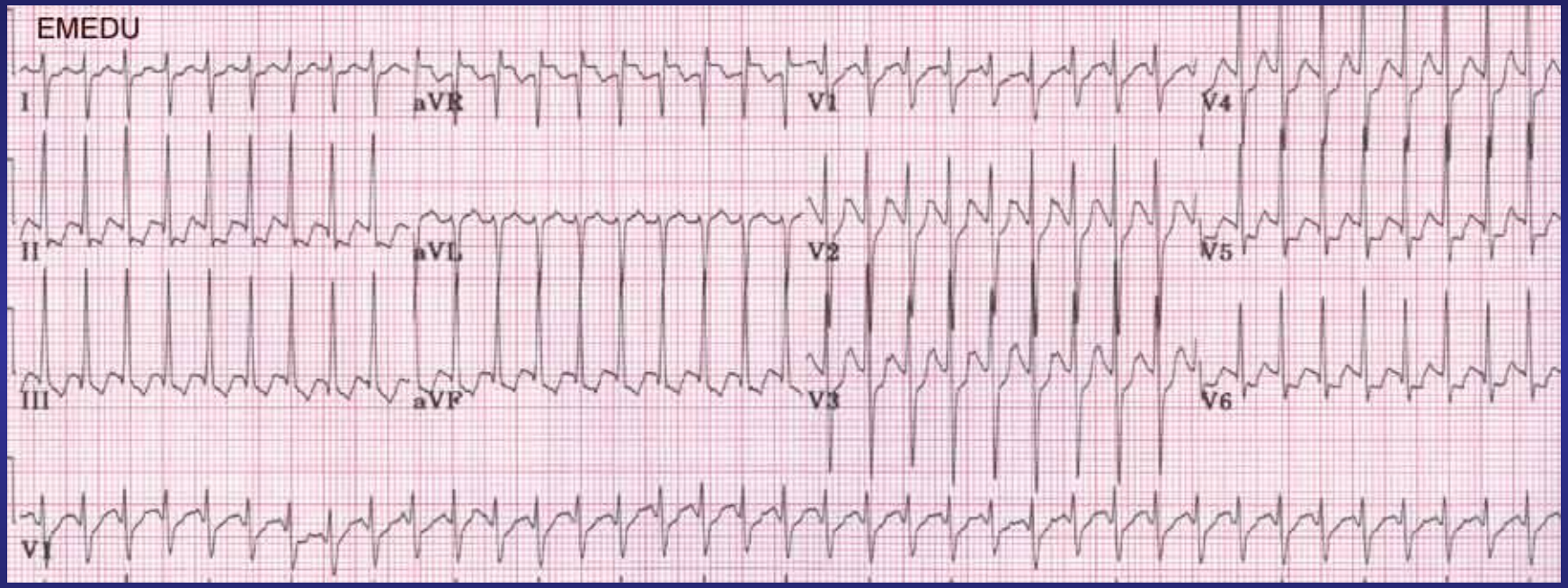

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6

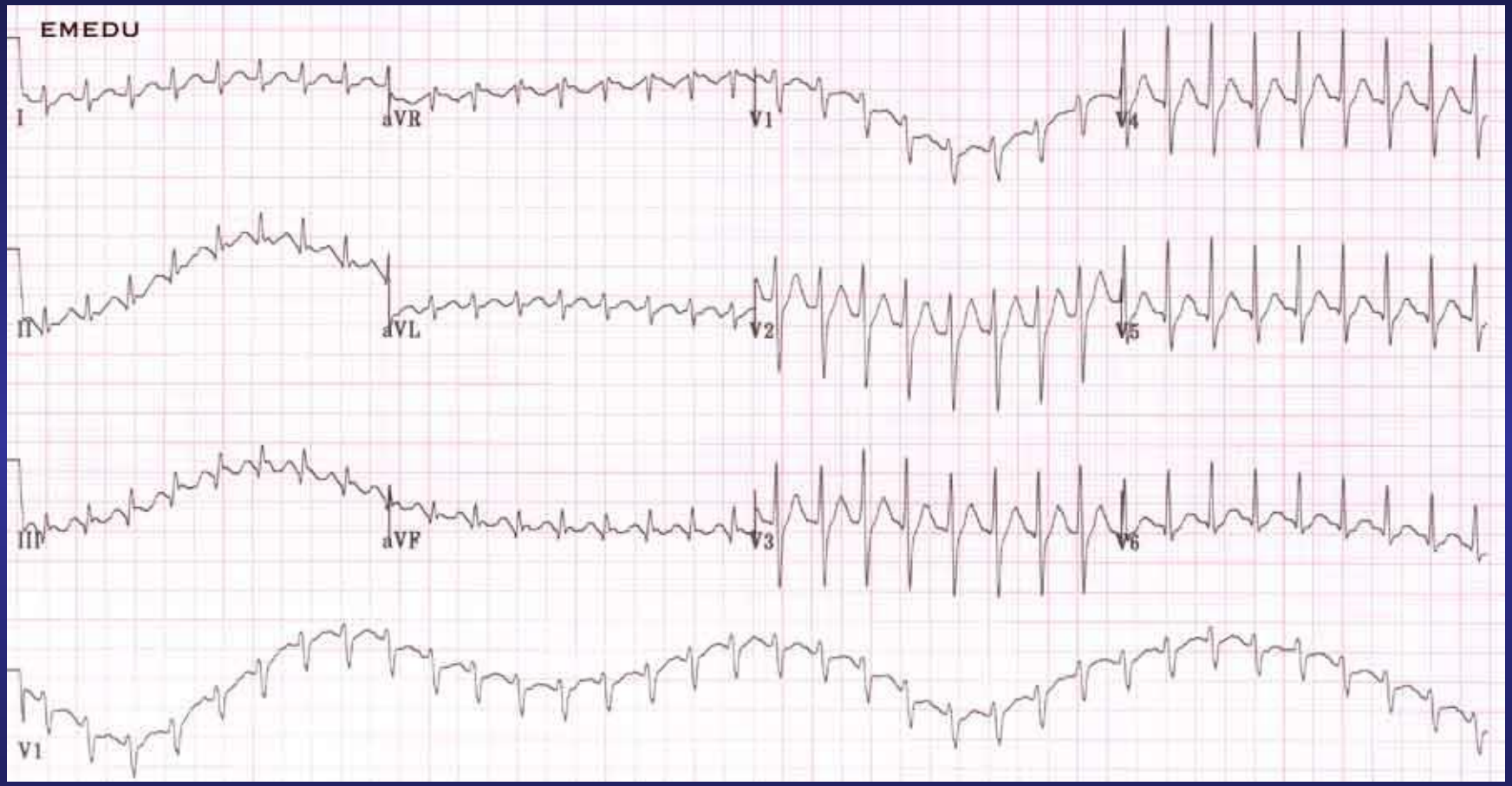

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6
V1

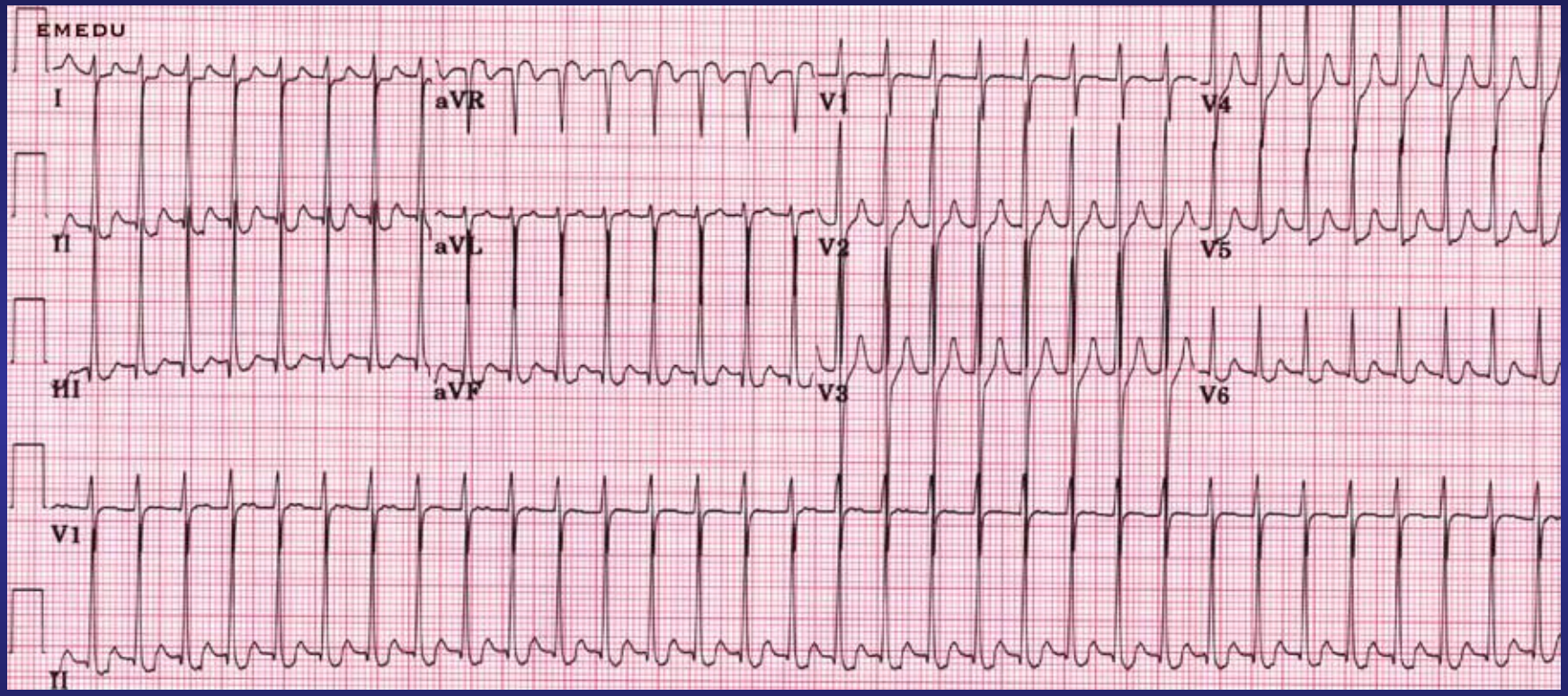

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6

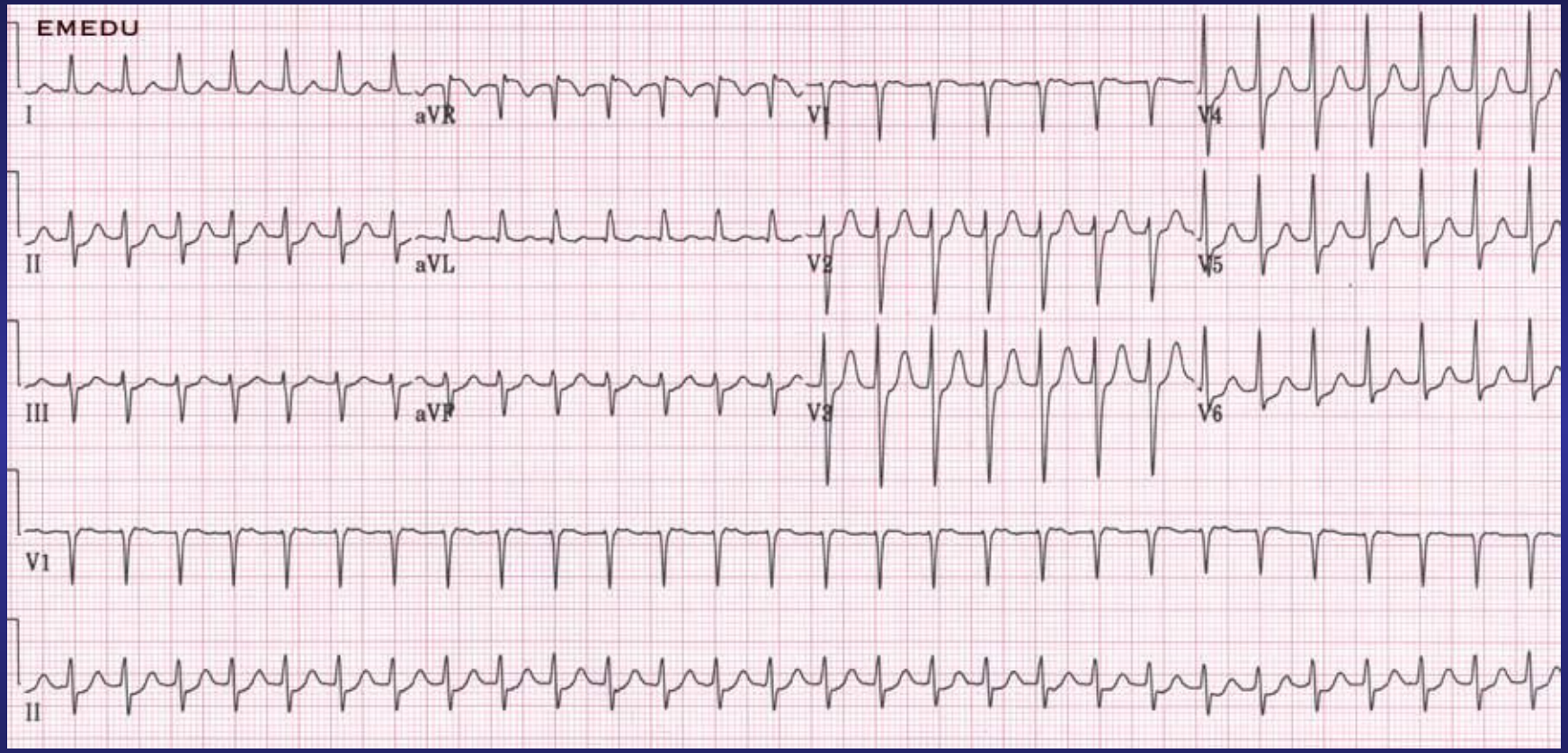

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6

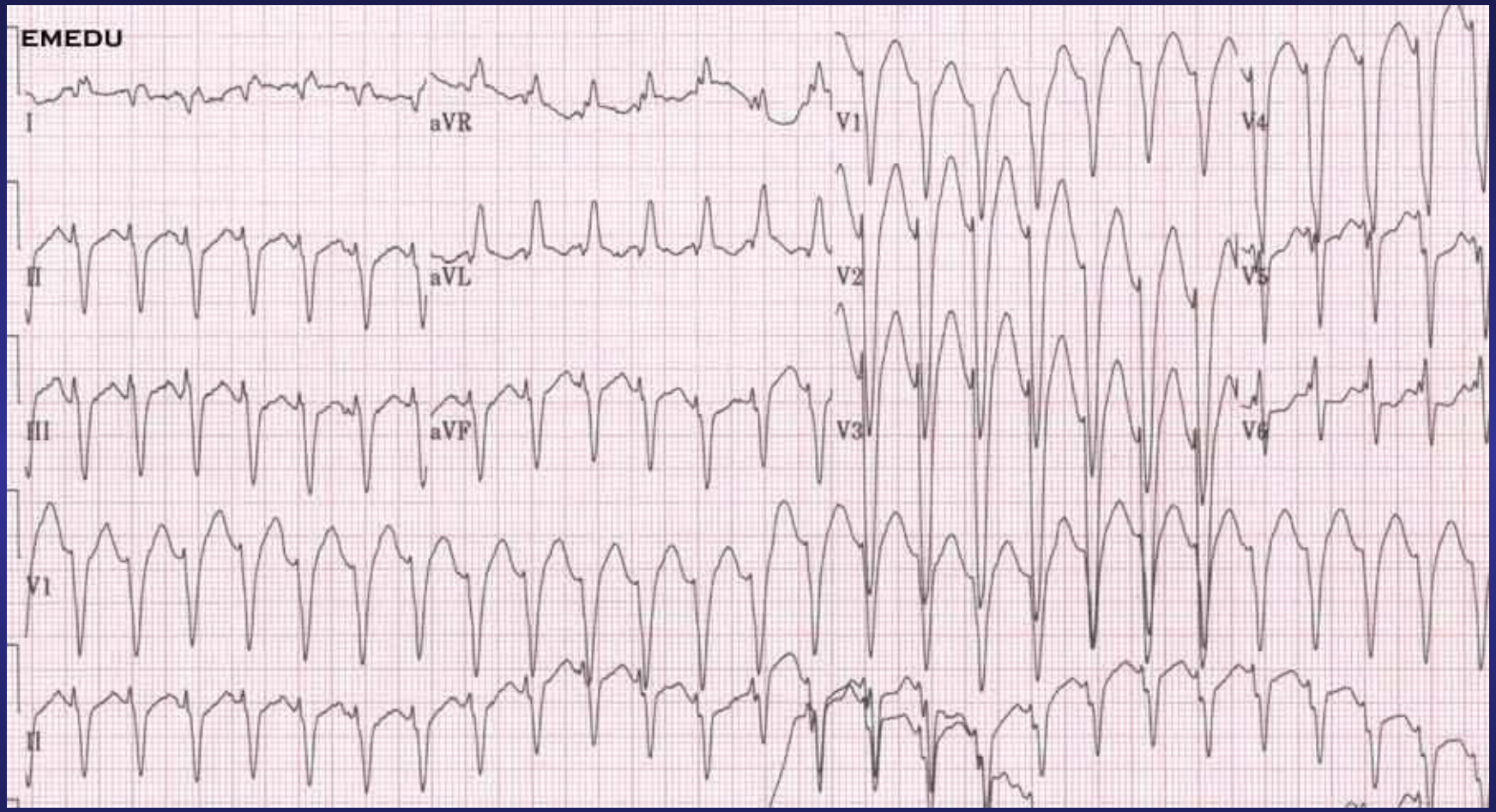

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6
V1

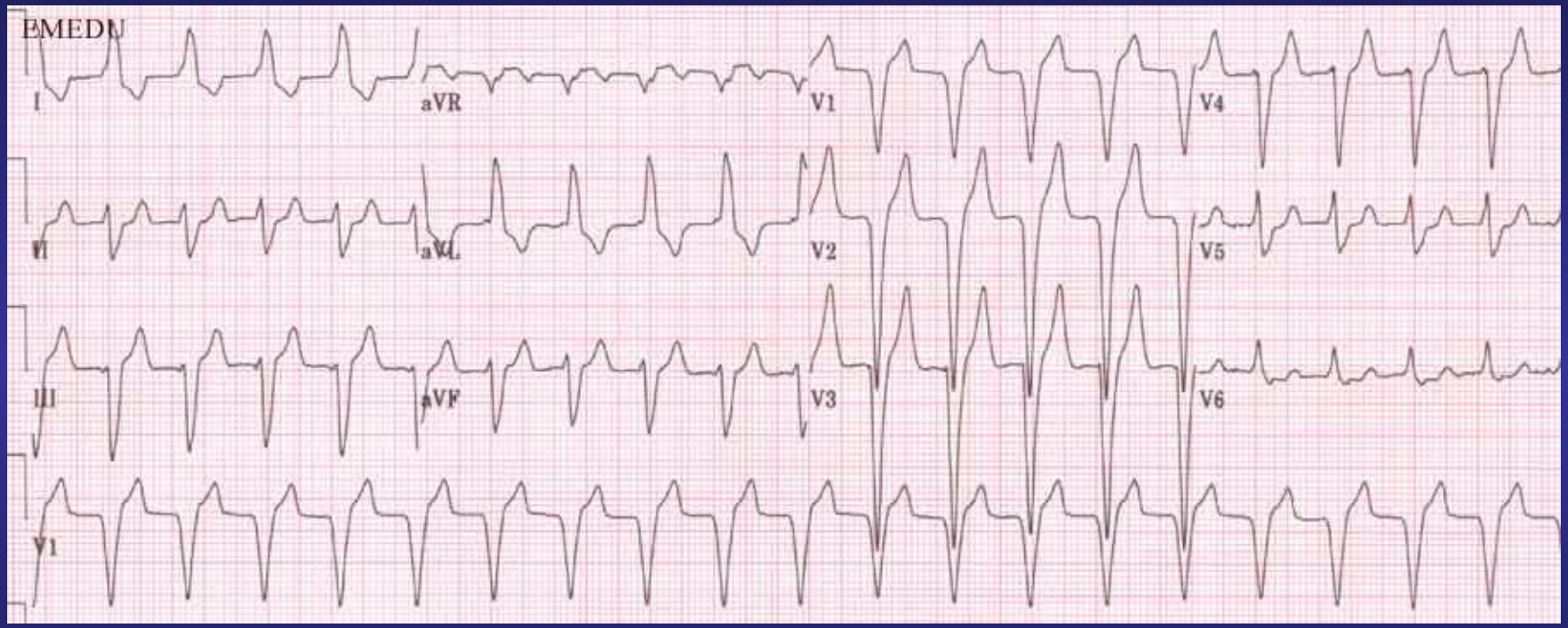

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6
V1

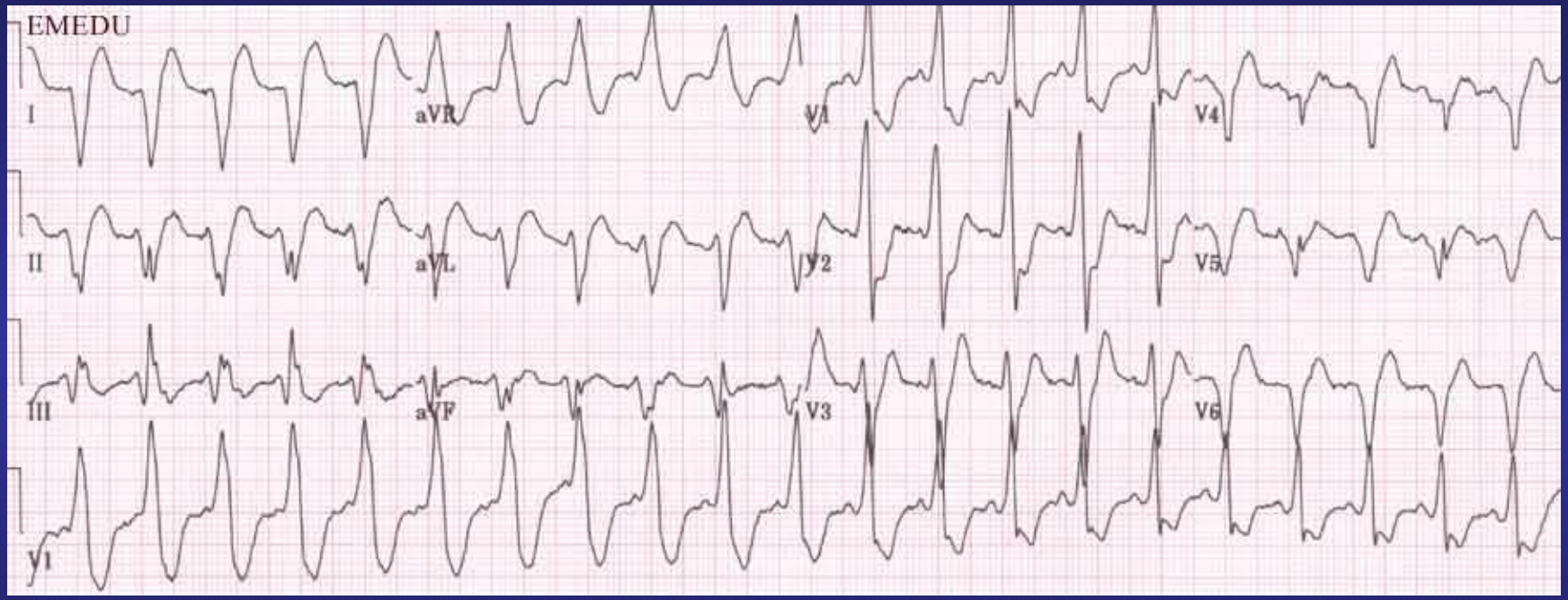

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6
V1

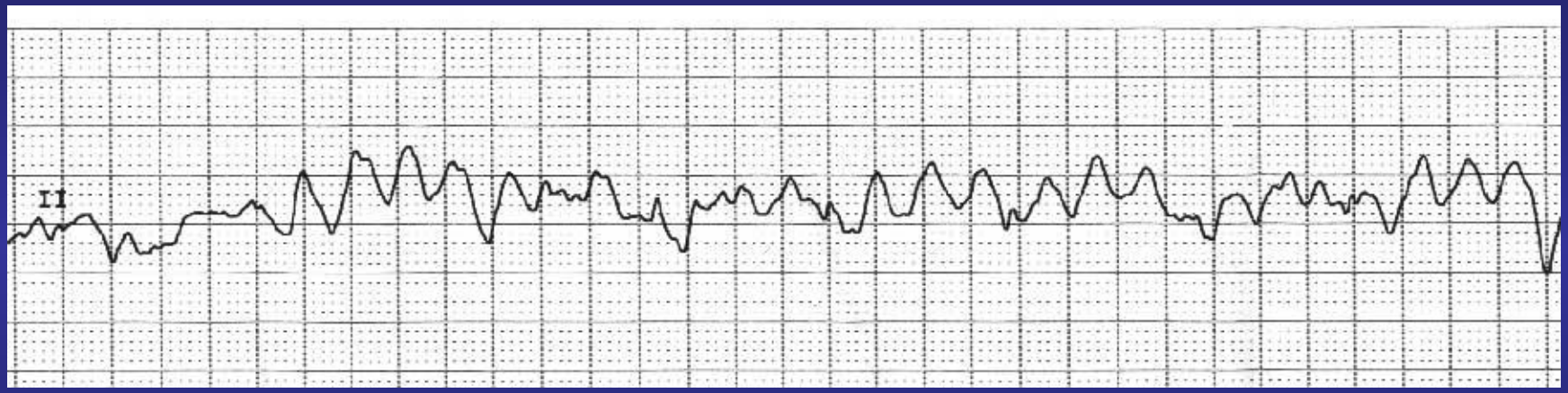

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6
V1
II

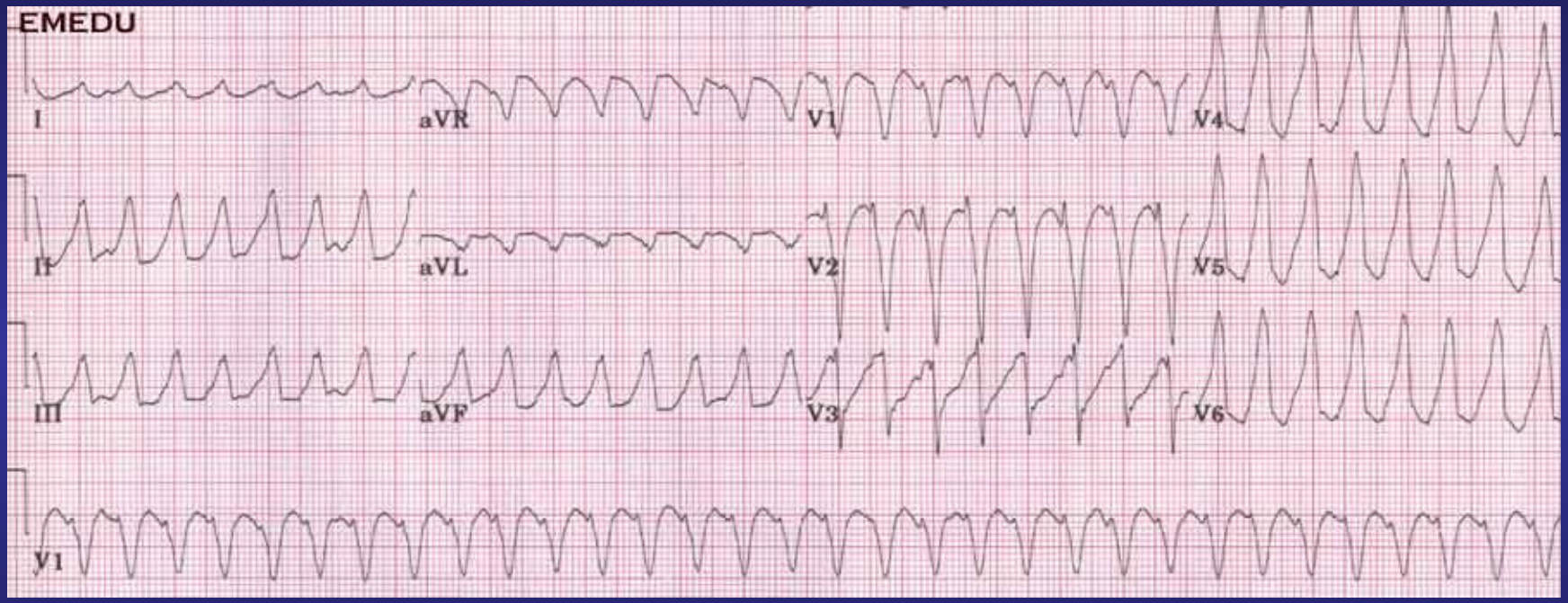

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6
V1
II


EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6
V1
II

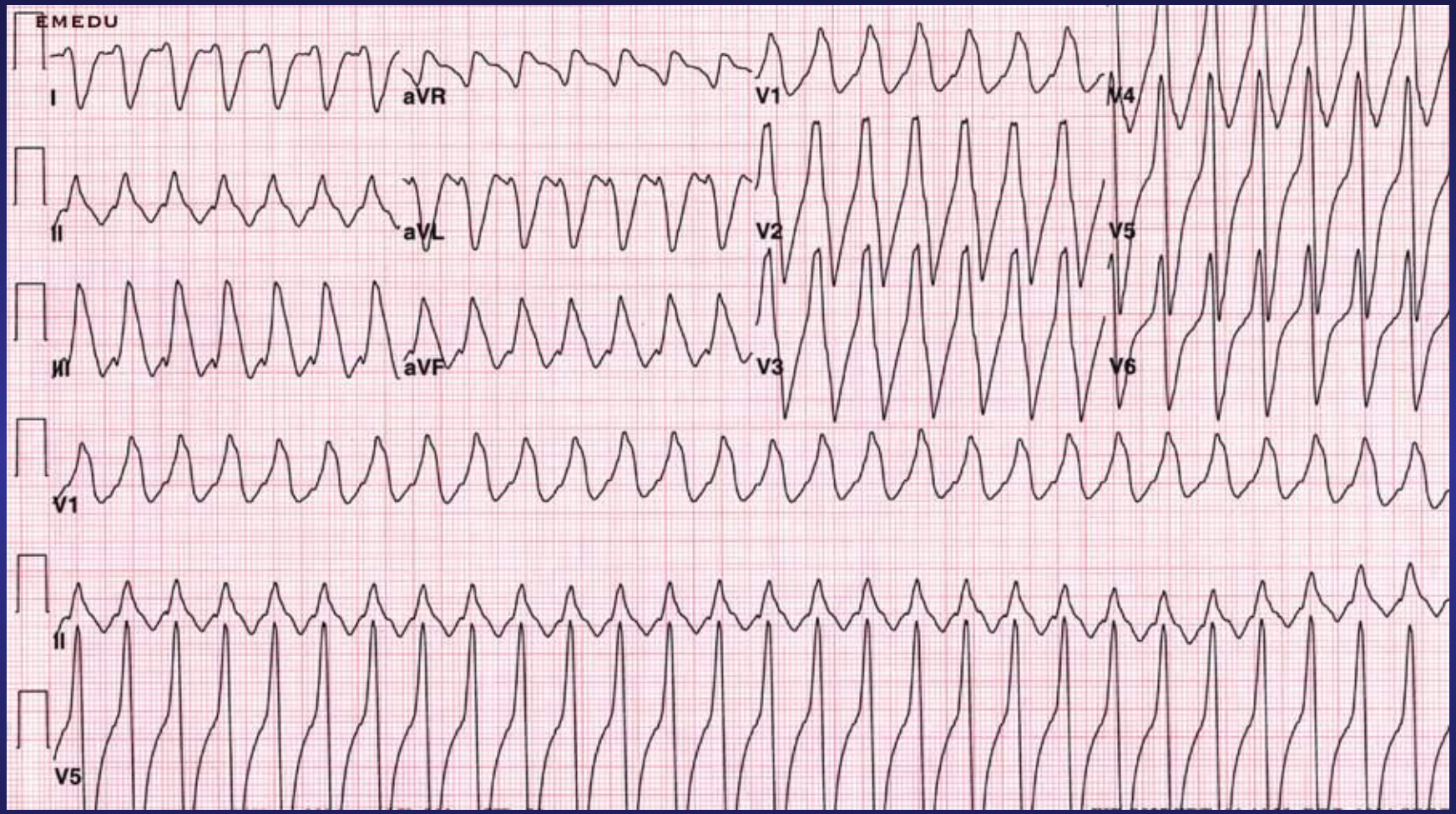

EMEDN
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6
V1

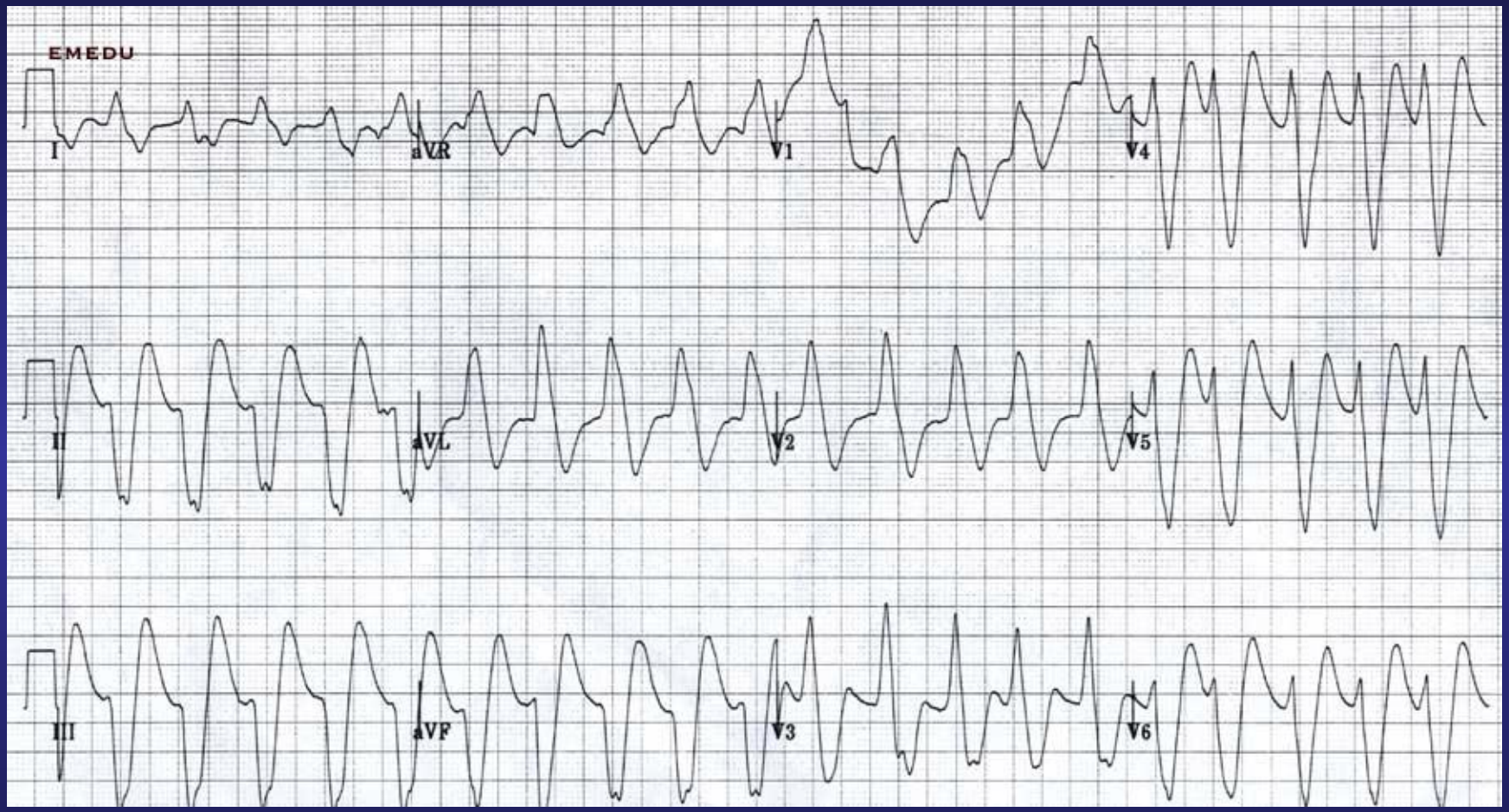

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6
y1

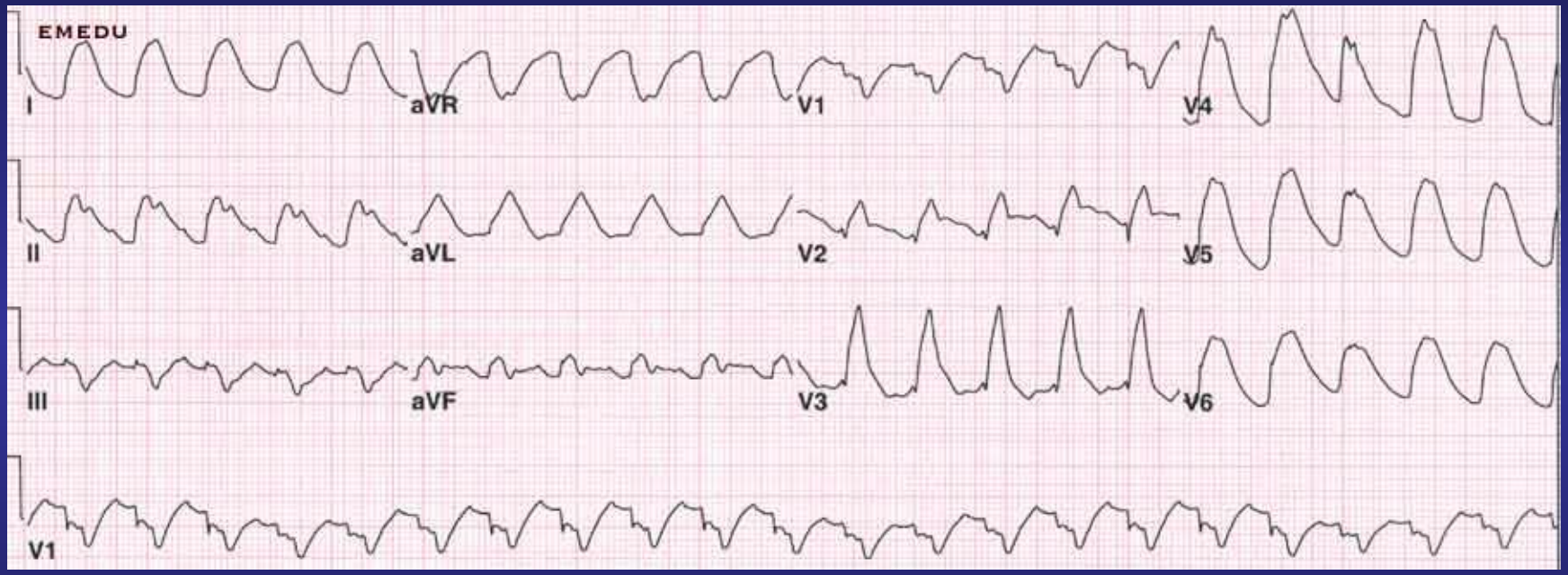

II

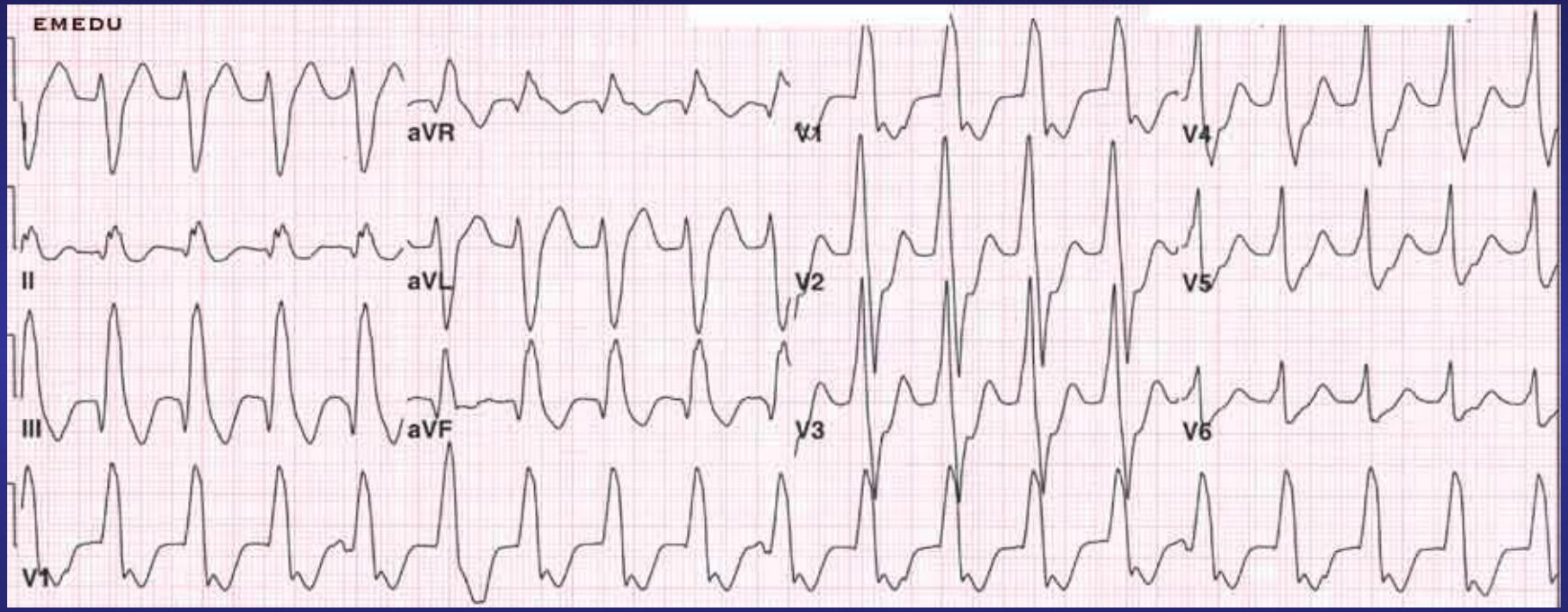

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6
V1

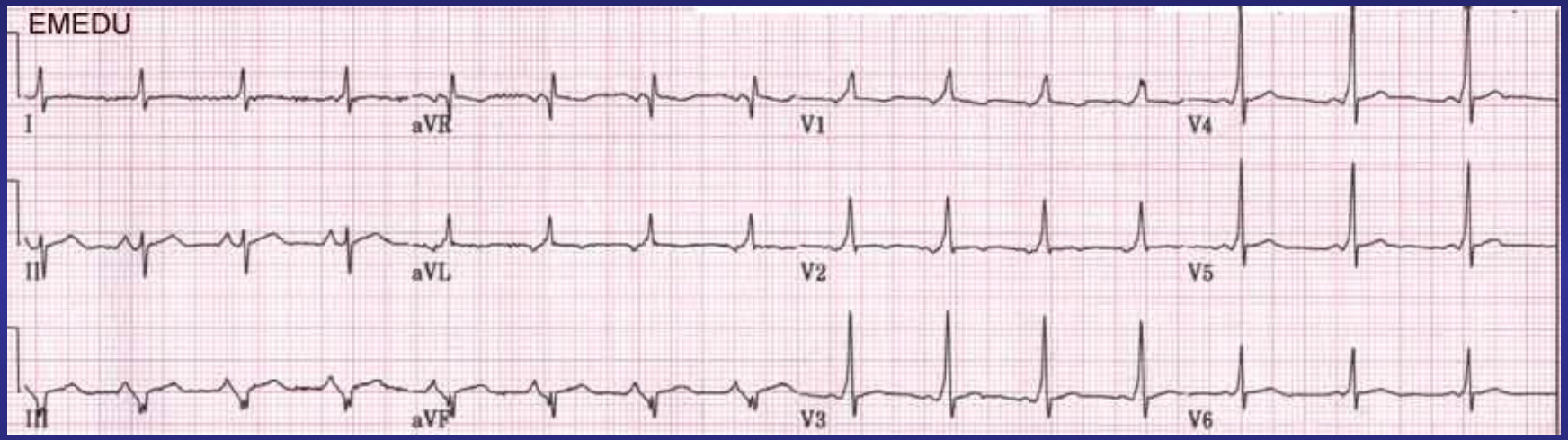

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6
V1
II

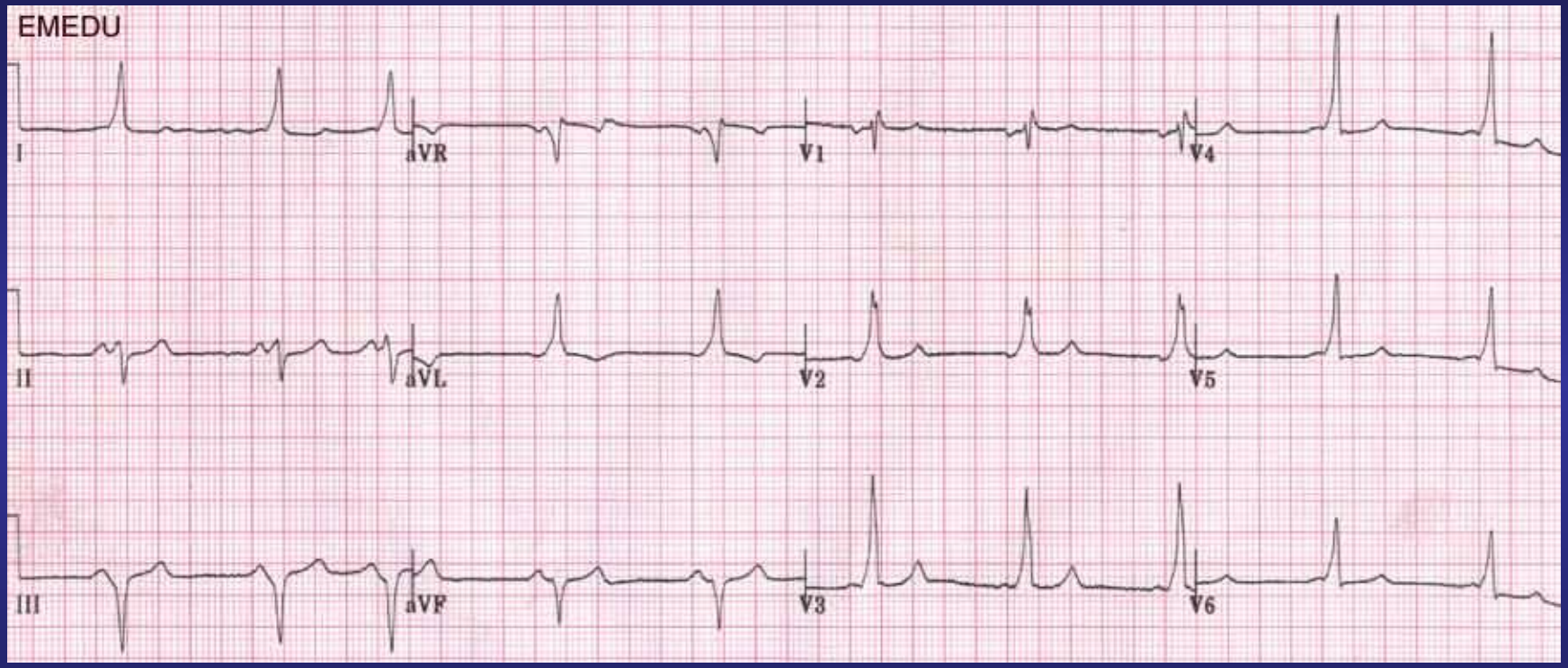

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6
V1
II
V5

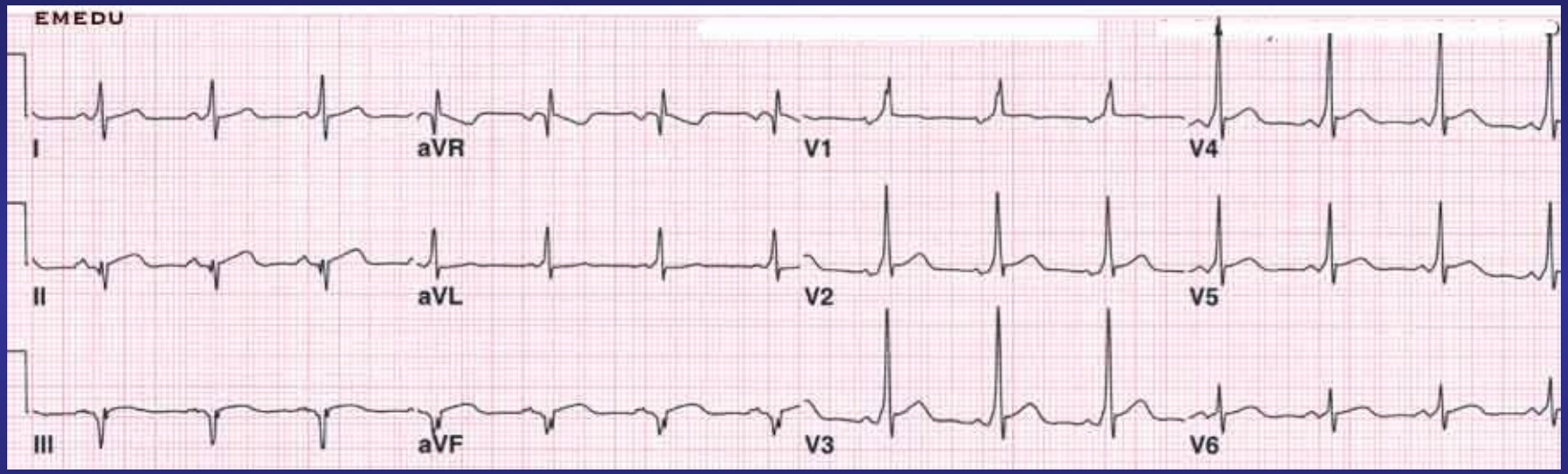

EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6


EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6
V1


EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6
V1


EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6


EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6


EMEDU
I
aVR
V1
V4
II
aVL
V2
V5
III
aVF
V3
V6